Amendment history of SSD1286 Product Proposal

Revision	Description of any change	Issued	Effective
0.10 22 Sep 03	Initial release	Alfred Au	-
0.20 16 Jan 04	Modified datasheet format	Natalie Tse	-
0.30 2 Feb 04	P.4 Revised the mapping for PS0-3. P.5 Added the pin VCI1. P.5 Added the pin description for VCIX2G P.5 Modified the description for CDUM1. P.7-10 Modified the pad coordinates. P.13,15 Changed the “Device code read” to 1286h. P.45 Revised the diagram for “filtering and charge sharing capacitor”. And the diagram for Power Supply Pins Connections	Natalie Tse	-

SSD1286
TFT Smart Drivers

Product Proposal

Integrated TFT Power, Gate, Source Driver with built-in RAM CMOS

1 General Description

SSD1286 TFT Smart Driver is an all in one driver that integrated the power circuits, gate driver, source driver and RAM into single chip. It can drive a 262k color a-TFT panel with resolution of 132 RGB x 176.

It also integrated the controller function and consists of up to 52,272 bytes (132 x 176 x 18 / 8) Graphic Display Data RAM (GDDRAM) such that it interfaced with common MCU through 8/9/16/18-bits 6800-series / 8080-series compatible Parallel Interface or Serial Interface and stored the data in the GDDRAM. Auxiliary 18-bits video interface (VSYNC, HSYNC, DOTCLK, ENABLE and PD0-17) are integrated into SSD1286 for displays animated image.

With down to 11 external capacitors only, it embeds DC-DC Converter, Oscillator and Voltage generator to provide all necessary voltage required by the driver with minimum external components. A Common Voltage Generation Circuit is included to drive the TFT-display counter electrode. An Integrated Gamma Control Circuit is also included that can be adjusted by software commands to provide maximum flexibility and optimal display quality.

It can be operated down to 1.16V and provide different power save modes. It is suitable for any portable battery-driven applications requiring long operation period with compact size.

SOLOMON SYSTECH

2 FEATURES

- Power Supply: V_{DD} = 1.65 V – 2.5V (non-regulated input for logic)
  V_{DDIO} = 1.16 V – 3.6V (regulated input for logic)
  V_{DDEXT} = 1.65 V – 3.6V (auxiliary input for logic when V_{DDIO} < 1.65 V)
  V_{CI} = 2.5V – 3.6V (power supply for internal analog circuit)
- Maximum Gate Driving Output Voltage : 30V p-p
- Maximum Source Driving Output Voltage : 5.5V
- Low Current Sleep Mode, Partial Display Mode and 8-colors Text Mode
- Display Size: 132 RGB x 176
- Display Color Support: 262k/65k colors a-TFT displays
- 8/9/16/18-bits 6800-series / 8080-series Parallel Interface, Serial Peripheral Interface
- 18-bit RGB-Interface for animated displays (VSYNC, HSYNC, DOTCLK, DEN, and PD0-17)
- On-Chip 52,272 bytes (132x176x18/8) Graphic Display Data RAM
- RAM write synchronization function
- Support Line and Frame Inversion
- Source and Gate scan direction control
- Software selection on Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- On-Chip DC-DC Converter up to 6x / -6x
- Typical Source Output Voltage variation : ±10 mV
- Programmable Common Electrode Voltage amplitude and level for both Cs on gate or Cs on common structure
- Programmable Gamma Correction Curve
- Programmable drive duty ratio up to 1/132 mux in steps of 1
- On-Chip Oscillator
- Non-Volatile Memory (OTP) for VCOM calibration
- Available in COG package with interlaced Gate Output in both sides

3 ORDERING INFORMATION

Table 1 - Ordering Information

Ordering Part Number	SEG (x RGB)	COM	Package Form	Reference
SSD1286Z	132	176	Gold Bump Die	

4 BLOCK DIAGRAM

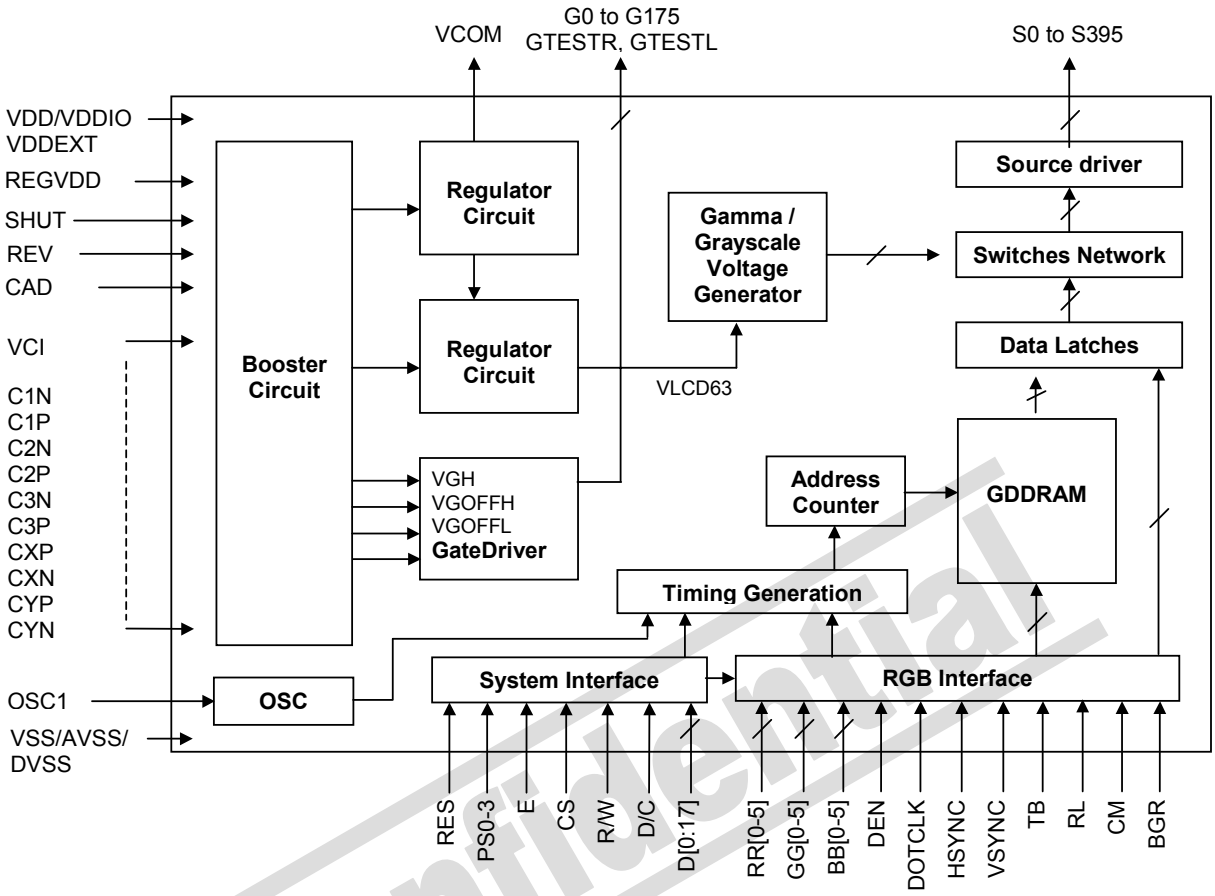


Figure 1. SSD1286 Block diagram Description.

5 PIN ASSIGNMENT

Table 2 – SSD1286 pin assignments

Name	Type	Function
CM	I	Input pin to select 262k-color or 8-color display mode. After entered 8-color mode, the driver will changed from line inversion to frame inversion mode, and only MSB of the data Red, Green and Blue will be considered.
RR5-0	I	Graphic Data Input Pins: Red Data – 6-bits Green Data – 6-bits Blue Data – 6-bits
GG5-0	I	
BB5-0	I	
DEN	I	Display enable pin from controller.
VSYNC	I	Frame synchronization signal. Fixed to VDD or VSS if not used.
HSYNC	I	Line synchronization signal. Fixed to VDD or VSS if not used.
DOTCLK	I	Dot-clock signal and oscillator source. External clock must be provided to that pin even at front or black porch non-display period.
SHUT	I	Display shut down pin in generic display mode. The driver will be put into sleep mode when SHUT = VDDIO and register R03h Dmode1-0 = 01h.
RL	I	Source driver data shift direction. First RGB data will be displayed at S0~S2 if connected to VDDIO. First RGB data will be displayed at S393-S395 if connected to VSS.
TB	I	Gate driver scan direction. Gate scan from G0 to G175 if connected to VDDIO; Gate scan from G175 to G0 if connected to VSS.
BGR	I	Color mapping selection pin. Refer to S0-S395 pin description.
REV	I	Display reverse selection pin. Display data 0 will be mapped to minimum pixel voltage if connected to VSS; Display data 0 will be mapped to maximum pixel voltage if connected to VDDIO.
CAD	I	Panel structure selection pin. Connect to VSS if Cs on common structure is used. Connect to VDDIO if Cs on gate structure is used.
PS0	I	PS(3:0) = 1111 : 3-wires MCU Serial interface 1110 : 4-wires MCU Serial interface 1011 : 16 bits 68 parallel interface 1010 : 8 bits 68 parallel interface 1001 : 16 bits 80 parallel interface 1000 : 8 bits 80 parallel interface 0111 : 18 bits 68 parallel interface 0110 : 9 bits 68 parallel interface 0101 : 18 bits 80 parallel interface 0100 : 9 bits 80 parallel interface
PS1	I	
PS2	I	
PS3	I	
D/C	I	Data or command
E; /WR	I	68-system : E (enable signal) 80-system : /WR (read strobe signal) Serial mode : Not used and should be connected to Vss
R/W; /RD	I	68-system : R/W (indicates read cycle when High, write cycle when Low) 80-system : /RD read strobe signal) Serial mode : Not used and should be connected to Vss
D0-D14	I/O	For parallel mode, 8/9/16/18 bit interface, refer to Section 14 Interface Mapping (P.38) for definition. For serial mode, D15-D17 are used. Unused pins should be connected to Vss
D15 (SDO)		
D16 (SCK)	I	
D17 (SDI)	I	
REGVDD	I	Internal VDD regulator control signal. When connected to VDDIO, internal VDD regulator will be ON when VDDEXT <= 2.0V, and VDDEXT will be connected to VDD internally. When connected to VSS, internal regulator will be OFF regardless of VDDEXT, and VDDEXT and VDD will not be internally connected. For normal operation, connect REGVDD to VSS if system VDD is below 2.5V, and connect REGVDD to VDDIO if system VDD is above 2.5V.
RES	I	System reset pin. Initialization occurs once this pin is pulled low, the minimum pulse length is 10us. A low pulse must be applied after power-on. Connect this pin to VDDIO when not used.
CS	I	Chip select pin.
VDD	Power	Voltage input pin for internal logic. System VDD > 2.5V : DO NOT connect VDD to system VDD and connect VDD to a 1uF **capacitor**. VDDEXT = VDDIO = system VDD 1.65V ≤ System VDD < 2.5V : VDD = VDDEXT = VDDIO = system VDD (VDDEXT will be internally shorted to VDD if VDDEXT < 2.0V) 1.16V ≤ System VDD < 1.65V : Connect VDD and VDDEXT to a voltage between 1.65V to 2.5V.
VDDEXT	Power	
VDDIO	Power	Connect to system VDD.
VSS	Power	Connect to system ground
AVSS	Power	Connect to system ground
VSSRC	Power	Connect to system ground
VCHS	Power	Connect to system ground
VCI	Power	Booster input voltage pin. Connect to stable voltage source between 2.5 to 3.6V. Connect a

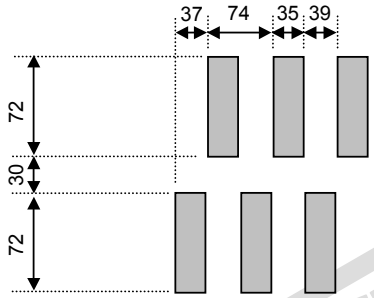
Name	Type	Function
		capacitor to VSS for stabilization.
VCI1	Power	For internal use only. Connect a **capacitor** to VSS
VCIP	Power	Connect to VCI
VCIX2	I	Short this pin to VCIX2G
VCIX2G	O	2 x VCI1, connect a **capacitor** for stabilization.
VCIM	I	A negative power output booster pin. Connect a **capacitor** for stabilization.
VCOMH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation.
VLCD63	O	This pin is the maximum source driver voltage.
VCOML	O	This pin indicates a low level of Vcom generated in driving the Vcom alternation. Leave this pin open.
VGH	O	A positive power output pin for gate driver. Connect a **capacitor** for stabilization
VGOFFL	O	A negative power output pin for gate driver. Connect a **capacitor** for stabilization
VGOFFH	O	When Cs on gate structure is used, this pin indicates a high level of Vgoff. Connect a **capacitor** for stabilization.
VGOFF	O	Connect a **capacitor** between VCOM and VGOFF
WSYNC	O	Ram Write Synchronization output
C1N	I	Connect a **capacitor** to C1P
C2N	I	Connect a **capacitor** to C2P
C3N	I	Connect a **capacitor** to C3P
C1P	I	Connect a **capacitor** to C1N
C2P	I	Connect a **capacitor** to C2N
C3P	I	Connect a **capacitor** to C3N
CXP	I	Connect a **capacitor** to CXN
CXN	I	Connect a **capacitor** to CXP
CYP	I	Connect a **capacitor** to CYN
CYN	I	Connect a **capacitor** to CYP
CDUM0	I	Charge recycling **capacitor** to VSS
CDUM1	I	Charge recycling **capacitor** to VSS
CDUM2	I	Test pin of the internal circuit. Leave open and insert test point in FPC.
TESTA	I	Test pin of the internal circuit. Leave open and insert test point in FPC.
TESTB	I	Test pin of the internal circuit. Leave open and insert test point in FPC.
TESTC	I	Test pin of the internal circuit. Leave open and insert test point in FPC.
VCOM	O	A power supply for the TFT-display common electrode. Connect a **capacitor** between VCOM and VGOFF.
OSC1	I	An internal oscillator reference pin, connect a resistor to VCI. Floating this pin when using the internal reference.
EXTCLK	I	A clock input pin for internal oscillator. Connect to VSS when using the internal oscillator.
GTESTR, GTESTL	O	Gate driver output test pins. Leave it disconnected when using Cs on Common structure
G0-G175	O	Gate driver output pins. This pin output either VGH, VgoffH or VgoffL level.
S0-S395	O	Source driver output pins. S(3n) : display Red if BGR = Low, Blue if BGR = High. S(3n+1) : display Green. S(3n+2) : display Blue if BGR = Low, Red if BGR = High.
NC		These pins must be left open and cannot be connected
DUMMY		Pins that are not connected inside the IC and floated. They can be connected to any voltage or shorted together.
TEST1~18		These pins must be left open and cannot be connected

6 DIE FLOOR PLAN (Gold bump face up)

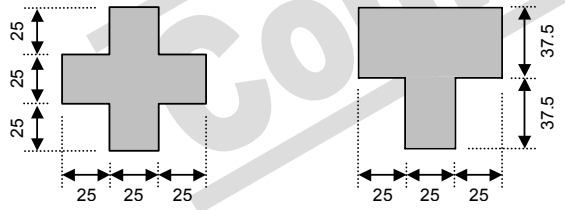
Die Information:

Die Size:	19770 x 2047 μm^2 (TBD)
Die Thickness:	406 ± 25μm
Bump Height:	15 μm (Typ.)
	Tolerance: < 3 μm within die
Bump size	
Pad 1-253	: 51 x 93 μm^2
Pad 256-291, 811-846	: 72 x 35 μm^2
Pad 296-806	: 35 x 72 μm^2
Pad 294-295, 807-808	: 49 x 72 μm^2
Pad 254-255, 292-293, 809-810, 847-848	: 72 x 49 μm^2
Minimum bump pitch	: 37 μm

Output Pad Pitch

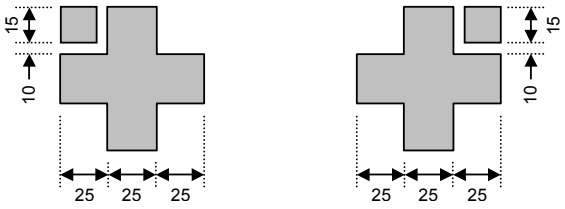


Alignment Marks:



Center: (x, y)
Size: 75 x 75 μm^2

Center: (x, y)
Size: 75 x 75 μm^2



Center: (x, y)
Size: 75 x 75 μm^2

Center: (x, y)
Size: 75 x 75 μm^2

7 Pin Assignment

Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos
1	NC	-9450	-742.5	213	VCHS	6450	-742.5	425	S321	4662	705	637	S114	-3182	705
2	NC	-9375	-742.5	214	VCHS	6525	-742.5	426	S320	4625	807	638	S113	-3219	807
3	VCOM	-9300	-742.5	215	VCHS	6600	-742.5	427	S319	4588	705	639	S112	-3256	705
4	VCOM	-9225	-742.5	216	VCHS	6675	-742.5	428	S318	4551	807	640	S111	-3293	807
5	VCOM	-9150	-742.5	217	CXP	6750	-742.5	429	S317	4514	705	641	S110	-3330	705
6	NC	-9075	-742.5	218	CXP	6825	-742.5	430	S316	4477	807	642	S109	-3367	807
7	NC	-9000	-742.5	219	CXP	6900	-742.5	431	S315	4440	705	643	S108	-3404	705
8	VGH	-8925	-742.5	220	CXN	6975	-742.5	432	S314	4403	807	644	S107	-3441	807
9	VGH	-8850	-742.5	221	CXN	7050	-742.5	433	S313	4366	705	645	S106	-3478	705
10	VGH	-8775	-742.5	222	CXN	7125	-742.5	434	S312	4329	807	646	S105	-3515	807
11	VCIX2	-8700	-742.5	223	VCI	7200	-742.5	435	S311	4292	705	647	S104	-3552	705
12	VCIX2	-8625	-742.5	224	VCI	7275	-742.5	436	S310	4255	807	648	S103	-3589	807
13	VCIX2	-8550	-742.5	225	VCI	7350	-742.5	437	S309	4218	705	649	S102	-3626	705
14	WSYNC	-8475	-742.5	226	VCI	7425	-742.5	438	S308	4181	807	650	S101	-3663	807
15	EXTCLK	-8400	-742.5	227	VCI	7500	-742.5	439	S307	4144	705	651	S100	-3700	705
16	VSS	-8325	-742.5	228	VCIX2	7575	-742.5	440	S306	4107	807	652	S99	-3737	807
17	REGVDD	-8250	-742.5	229	VCIX2	7650	-742.5	441	S305	4070	705	653	S98	-3774	705
18	VDDIO	-8175	-742.5	230	VCIX2	7725	-742.5	442	S304	4033	807	654	S97	-3811	807
19	CAD	-8100	-742.5	231	VCIX2	7800	-742.5	443	S303	3996	705	655	S96	-3848	705
20	BGR	-8025	-742.5	232	VCIX2	7875	-742.5	444	S302	3959	807	656	S95	-3885	807
21	REV	-7950	-742.5	233	VCIX2G	7950	-742.5	445	S301	3922	705	657	S94	-3922	705
22	PS0	-7875	-742.5	234	VCIX2G	8025	-742.5	446	S300	3885	807	658	S93	-3959	807
23	PS1	-7800	-742.5	235	VCIX2G	8100	-742.5	447	S299	3848	705	659	S92	-3996	705
24	PS2	-7725	-742.5	236	VCIX2G	8175	-742.5	448	S298	3811	807	660	S91	-4033	807
25	PS3	-7650	-742.5	237	CYP	8250	-742.5	449	S297	3774	705	661	S90	-4070	705
26	VSS	-7575	-742.5	238	CYP	8325	-742.5	450	S296	3737	807	662	S89	-4107	807
27	TB	-7500	-742.5	239	CYP	8400	-742.5	451	S295	3700	705	663	S88	-4144	705
28	VDDIO	-7425	-742.5	240	CYP	8475	-742.5	452	S294	3663	807	664	S87	-4181	807
29	RL	-7350	-742.5	241	CYP	8550	-742.5	453	S293	3626	705	665	S86	-4218	705
30	VSS	-7275	-742.5	242	CYN	8625	-742.5	454	S292	3589	807	666	S85	-4255	807
31	SHUT	-7200	-742.5	243	CYN	8700	-742.5	455	S291	3552	705	667	S84	-4292	705
32	VSYNC	-7125	-742.5	244	CYN	8775	-742.5	456	S290	3515	807	668	S83	-4329	807
33	VSYNC	-7050	-742.5	245	CYN	8850	-742.5	457	S289	3478	705	669	S82	-4366	705
34	HSYNC	-6975	-742.5	246	CYN	8925	-742.5	458	S288	3441	807	670	S81	-4403	807
35	HSYNC	-6900	-742.5	247	DUMMY	9000	-742.5	459	S287	3404	705	671	S80	-4440	705
36	DOTCLK	-6825	-742.5	248	DUMMY	9075	-742.5	460	S286	3367	807	672	S79	-4477	807
37	DOTCLK	-6750	-742.5	249	VCOM	9150	-742.5	461	S285	3330	705	673	S78	-4514	705
38	DEN	-6675	-742.5	250	VCOM	9225	-742.5	462	S284	3293	807	674	S77	-4551	807
39	DEN	-6600	-742.5	251	VCOM	9300	-742.5	463	S283	3256	705	675	S76	-4588	705
40	VDDIO	-6525	-742.5	252	NC	9375	-742.5	464	S282	3219	807	676	S75	-4625	807
41	RR5	-6450	-742.5	253	NC	9450	-742.5	465	S281	3182	705	677	S74	-4662	705
42	RR5	-6375	-742.5	254	DUMMY	9664	-732	466	S280	3145	807	678	S73	-4699	807
43	RR4	-6300	-742.5	255	DUMMY	9562	-681	467	S279	3108	705	679	S72	-4736	705
44	RR4	-6225	-742.5	256	G1	9664	-637	468	S278	3071	807	680	S71	-4773	807
45	RR3	-6150	-742.5	257	G3	9562	-600	469	S277	3034	705	681	S70	-4810	705
46	RR3	-6075	-742.5	258	G5	9664	-563	470	S276	2997	807	682	S69	-4847	807
47	RR2	-6000	-742.5	259	G7	9562	-526	471	S275	2960	705	683	S68	-4884	705
48	RR2	-5925	-742.5	260	G9	9664	-489	472	S274	2923	807	684	S67	-4921	807
49	RR1	-5850	-742.5	261	G11	9562	-452	473	S273	2886	705	685	S66	-4958	705
50	RR1	-5775	-742.5	262	G13	9664	-415	474	S272	2849	807	686	S65	-4995	807
51	RR0	-5700	-742.5	263	G15	9562	-378	475	S271	2812	705	687	S64	-5032	705
52	RR0	-5625	-742.5	264	G17	9664	-341	476	S270	2775	807	688	S63	-5069	807
53	GG5	-5550	-742.5	265	G19	9562	-304	477	S269	2738	705	689	S62	-5106	705
54	GG5	-5475	-742.5	266	G21	9664	-267	478	S268	2701	807	690	S61	-5143	807

Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos
55	GG4	-5400	-742.5	267	G23	9562	-230	479	S267	2664	705	691	S60	-5180	705
56	GG4	-5325	-742.5	268	G25	9664	-193	480	S266	2627	807	692	S59	-5217	807
57	GG3	-5250	-742.5	269	G27	9562	-156	481	S265	2590	705	693	S58	-5254	705
58	GG3	-5175	-742.5	270	G29	9664	-119	482	S264	2553	807	694	S57	-5291	807
59	GG2	-5100	-742.5	271	G31	9562	-82	483	S263	2516	705	695	S56	-5328	705
60	GG2	-5025	-742.5	272	G33	9664	-45	484	S262	2479	807	696	S55	-5365	807
61	GG1	-4950	-742.5	273	G35	9562	-8	485	S261	2442	705	697	S54	-5402	705
62	GG1	-4875	-742.5	274	G37	9664	29	486	S260	2405	807	698	S53	-5439	807
63	GG0	-4800	-742.5	275	G39	9562	66	487	S259	2368	705	699	S52	-5476	705
64	GG0	-4725	-742.5	276	G41	9664	103	488	S258	2331	807	700	S51	-5513	807
65	BB0	-4650	-742.5	277	G43	9562	140	489	S257	2294	705	701	S50	-5550	705
66	BB0	-4575	-742.5	278	G45	9664	177	490	S256	2257	807	702	S49	-5587	807
67	BB1	-4500	-742.5	279	G47	9562	214	491	S255	2220	705	703	S48	-5624	705
68	BB1	-4425	-742.5	280	G49	9664	251	492	S254	2183	807	704	S47	-5661	807
69	BB2	-4350	-742.5	281	G51	9562	288	493	S253	2146	705	705	S46	-5698	705
70	BB2	-4275	-742.5	282	G53	9664	325	494	S252	2109	807	706	S45	-5735	807
71	BB3	-4200	-742.5	283	G55	9562	362	495	S251	2072	705	707	S44	-5772	705
72	BB3	-4125	-742.5	284	G57	9664	399	496	S250	2035	807	708	S43	-5809	807
73	BB4	-4050	-742.5	285	G59	9562	436	497	S249	1998	705	709	S42	-5846	705
74	BB4	-3975	-742.5	286	G61	9664	473	498	S248	1961	807	710	S41	-5883	807
75	BB5	-3900	-742.5	287	G63	9562	510	499	S247	1924	705	711	S40	-5920	705
76	BB5	-3825	-742.5	288	G65	9664	547	500	S246	1887	807	712	S39	-5957	807
77	CM	-3750	-742.5	289	G67	9562	584	501	S245	1850	705	713	S38	-5994	705
78	D0	-3675	-742.5	290	G69	9664	621	502	S244	1813	807	714	S37	-6031	807
79	D1	-3600	-742.5	291	G71	9562	658	503	S243	1776	705	715	S36	-6068	705
80	D2	-3525	-742.5	292	DUMMY	9664	702	504	S242	1739	807	716	S35	-6105	807
81	D3	-3450	-742.5	293	DUMMY	9664	775	505	S241	1702	705	717	S34	-6142	705
82	D4	-3375	-742.5	294	DUMMY	9574	807	506	S240	1665	807	718	S33	-6179	807
83	D5	-3300	-742.5	295	DUMMY	9501	807	507	S239	1628	705	719	S32	-6216	705
84	D6	-3225	-742.5	296	G73	9435	807	508	S238	1591	807	720	S31	-6253	807
85	D7	-3150	-742.5	297	G75	9398	705	509	S237	1554	705	721	S30	-6290	705
86	D8	-3075	-742.5	298	G77	9361	807	510	S236	1517	807	722	S29	-6327	807
87	E	-3000	-742.5	299	G79	9324	705	511	S235	1480	705	723	S28	-6364	705
88	RW	-2925	-742.5	300	G81	9287	807	512	S234	1443	807	724	S27	-6401	807
89	DC	-2850	-742.5	301	G83	9250	705	513	S233	1406	705	725	S26	-6438	705
90	VSS	-2775	-742.5	302	G85	9213	807	514	S232	1369	807	726	S25	-6475	807
91	D9	-2700	-742.5	303	G87	9176	705	515	S231	1332	705	727	S24	-6512	705
92	D10	-2625	-742.5	304	G89	9139	807	516	S230	1295	807	728	S23	-6549	807
93	D11	-2550	-742.5	305	G91	9102	705	517	S229	1258	705	729	S22	-6586	705
94	D12	-2475	-742.5	306	G93	9065	807	518	S228	1221	807	730	S21	-6623	807
95	D13	-2400	-742.5	307	G95	9028	705	519	S227	1184	705	731	S20	-6660	705
96	D14	-2325	-742.5	308	G97	8991	807	520	S226	1147	807	732	S19	-6697	807
97	D15	-2250	-742.5	309	G99	8954	705	521	S225	1110	705	733	S18	-6734	705
98	D16	-2175	-742.5	310	G101	8917	807	522	S224	1073	807	734	S17	-6771	807
99	D17	-2100	-742.5	311	G103	8880	705	523	S223	1036	705	735	S16	-6808	705
100	RES	-2025	-742.5	312	G105	8843	807	524	S222	999	807	736	S15	-6845	807
101	CS	-1950	-742.5	313	G107	8806	705	525	S221	962	705	737	S14	-6882	705
102	CDUM0	-1875	-742.5	314	G109	8769	807	526	S220	925	807	738	S13	-6919	807
103	CDUM0	-1800	-742.5	315	G111	8732	705	527	S219	888	705	739	S12	-6956	705
104	CDUM0	-1725	-742.5	316	G113	8695	807	528	S218	851	807	740	S11	-6993	807
105	CDUM1	-1650	-742.5	317	G115	8658	705	529	S217	814	705	741	S10	-7030	705
106	CDUM1	-1575	-742.5	318	G117	8621	807	530	S216	777	807	742	S9	-7067	807
107	CDUM2	-1500	-742.5	319	G119	8584	705	531	S215	740	705	743	S8	-7104	705
108	TEST1	-1425	-742.5	320	G121	8547	807	532	S214	703	807	744	S7	-7141	807
109	TEST2	-1350	-742.5	321	G123	8510	705	533	S213	666	705	745	S6	-7178	705
110	TEST3	-1275	-742.5	322	G125	8473	807	534	S212	629	807	746	S5	-7215	807
111	TEST4	-1200	-742.5	323	G127	8436	705	535	S211	592	705	747	S4	-7252	705

Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos
112	TEST5	-1125	-742.5	324	G129	8399	807	536	S210	555	807	748	S3	-7289	807
113	TEST6	-1050	-742.5	325	G131	8362	705	537	S209	518	705	749	S2	-7326	705
114	TEST7	-975	-742.5	326	G133	8325	807	538	S208	481	807	750	S1	-7363	807
115	TEST8	-900	-742.5	327	G135	8288	705	539	S207	444	705	751	S0	-7400	705
116	VSS	-825	-742.5	328	G137	8251	807	540	S206	407	807	752	DUMMY	-7437	807
117	TEST9	-750	-742.5	329	G139	8214	705	541	S205	370	705	753	DUMMY	-7474	705
118	TEST10	-675	-742.5	330	G141	8177	807	542	S204	333	807	754	G174	-7511	807
119	TEST11	-600	-742.5	331	G143	8140	705	543	S203	296	705	755	G172	-7548	705
120	TEST12	-525	-742.5	332	G145	8103	807	544	S202	259	807	756	G170	-7585	807
121	TEST13	-450	-742.5	333	G147	8066	705	545	S201	222	705	757	G168	-7622	705
122	TEST14	-375	-742.5	334	G149	8029	807	546	S200	185	807	758	G166	-7659	807
123	TEST15	-300	-742.5	335	G151	7992	705	547	S199	148	705	759	G164	-7696	705
124	TEST16	-225	-742.5	336	G153	7955	807	548	S198	111	807	760	G162	-7733	807
125	TEST17	-150	-742.5	337	G155	7918	705	549	DUMMY	74	705	761	G160	-7770	705
126	TEST18	-75	-742.5	338	G157	7881	807	550	DUMMY	37	807	762	G158	-7807	807
127	TESTA	0	-742.5	339	G159	7844	705	551	DUMMY	0	705	763	G156	-7844	705
128	TESTB	75	-742.5	340	G161	7807	807	552	DUMMY	-37	807	764	G154	-7881	807
129	VLCD63	150	-742.5	341	G163	7770	705	553	DUMMY	-74	705	765	G152	-7918	705
130	VLCD63	225	-742.5	342	G165	7733	807	554	S197	-111	807	766	G150	-7955	807
131	NC	300	-742.5	343	G167	7696	705	555	S196	-148	705	767	G148	-7992	705
132	VSSRC	375	-742.5	344	G169	7659	807	556	S195	-185	807	768	G146	-8029	807
133	VSSRC	450	-742.5	345	G171	7622	705	557	S194	-222	705	769	G144	-8066	705
134	NC	525	-742.5	346	G173	7585	807	558	S193	-259	807	770	G142	-8103	807
135	VSS	600	-742.5	347	G175	7548	705	559	S192	-296	705	771	G140	-8140	705
136	VSS	675	-742.5	348	GTESTR	7511	807	560	S191	-333	807	772	G138	-8177	807
137	VSS	750	-742.5	349	DUMMY	7474	705	561	S190	-370	705	773	G136	-8214	705
138	VSS	825	-742.5	350	DUMMY	7437	807	562	S189	-407	807	774	G134	-8251	807
139	NC	900	-742.5	351	S395	7400	705	563	S188	-444	705	775	G132	-8288	705
140	AVSS	975	-742.5	352	S394	7363	807	564	S187	-481	807	776	G130	-8325	807
141	AVSS	1050	-742.5	353	S393	7326	705	565	S186	-518	705	777	G128	-8362	705
142	AVSS	1125	-742.5	354	S392	7289	807	566	S185	-555	807	778	G126	-8399	807
143	AVSS	1200	-742.5	355	S391	7252	705	567	S184	-592	705	779	G124	-8436	705
144	NC	1275	-742.5	356	S390	7215	807	568	S183	-629	807	780	G122	-8473	807
145	OSC1	1350	-742.5	357	S389	7178	705	569	S182	-666	705	781	G120	-8510	705
146	VCI	1425	-742.5	358	S388	7141	807	570	S181	-703	807	782	G118	-8547	807
147	VCI	1500	-742.5	359	S387	7104	705	571	S180	-740	705	783	G116	-8584	705
148	VCIP	1575	-742.5	360	S386	7067	807	572	S179	-777	807	784	G114	-8621	807
149	VCIP	1650	-742.5	361	S385	7030	705	573	S178	-814	705	785	G112	-8658	705
150	VDDEXT	1725	-742.5	362	S384	6993	807	574	S177	-851	807	786	G110	-8695	807
151	VDDEXT	1800	-742.5	363	S383	6956	705	575	S176	-888	705	787	G108	-8732	705
152	VDD	1875	-742.5	364	S382	6919	807	576	S175	-925	807	788	G106	-8769	807
153	VDD	1950	-742.5	365	S381	6882	705	577	S174	-962	705	789	G104	-8806	705
154	VDD	2025	-742.5	366	S380	6845	807	578	S173	-999	807	790	G102	-8843	807
155	NC	2100	-742.5	367	S379	6808	705	579	S172	-1036	705	791	G100	-8880	705
156	VDDIO	2175	-742.5	368	S378	6771	807	580	S171	-1073	807	792	G98	-8917	807
157	VDDIO	2250	-742.5	369	S377	6734	705	581	S170	-1110	705	793	G96	-8954	705
158	VCOMH	2325	-742.5	370	S376	6697	807	582	S169	-1147	807	794	G94	-8991	807
159	VCOMH	2400	-742.5	371	S375	6660	705	583	S168	-1184	705	795	G92	-9028	705
160	VCOMH	2475	-742.5	372	S374	6623	807	584	S167	-1221	807	796	G90	-9065	807
161	NC	2550	-742.5	373	S373	6586	705	585	S166	-1258	705	797	G88	-9102	705
162	VGOFF	2625	-742.5	374	S372	6549	807	586	S165	-1295	807	798	G86	-9139	807
163	VGOFF	2700	-742.5	375	S371	6512	705	587	S164	-1332	705	799	G84	-9176	705
164	VGOFF	2775	-742.5	376	S370	6475	807	588	S163	-1369	807	800	G82	-9213	807
165	VGOFFH	2850	-742.5	377	S369	6438	705	589	S162	-1406	705	801	G80	-9250	705
166	VGOFFH	2925	-742.5	378	S368	6401	807	590	S161	-1443	807	802	G78	-9287	807
167	VGOFFH	3000	-742.5	379	S367	6364	705	591	S160	-1480	705	803	G76	-9324	705
168	VCOML	3075	-742.5	380	S366	6327	807	592	S159	-1517	807	804	G74	-9361	807

Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos	Pin	Pin name	x-pos	y-pos
169	VCOML	3150	-742.5	381	S365	6290	705	593	S158	-1554	705	805	G72	-9398	705
170	AVSS	3225	-742.5	382	S364	6253	807	594	S157	-1591	807	806	G70	-9435	807
171	C1P	3300	-742.5	383	S363	6216	705	595	S156	-1628	705	807	DUMMY	-9501	807
172	C1P	3375	-742.5	384	S362	6179	807	596	S155	-1665	807	808	DUMMY	-9574	807
173	C1P	3450	-742.5	385	S361	6142	705	597	S154	-1702	705	809	DUMMY	-9664	775
174	C1P	3525	-742.5	386	S360	6105	807	598	S153	-1739	807	810	DUMMY	-9664	702
175	C1N	3600	-742.5	387	S359	6068	705	599	S152	-1776	705	811	G68	-9562	658
176	C1N	3675	-742.5	388	S358	6031	807	600	S151	-1813	807	812	G66	-9664	621
177	C1N	3750	-742.5	389	S357	5994	705	601	S150	-1850	705	813	G64	-9562	584
178	C1N	3825	-742.5	390	S356	5957	807	602	S149	-1887	807	814	G62	-9664	547
179	TESTC	3900	-742.5	391	S355	5920	705	603	S148	-1924	705	815	G60	-9562	510
180	C2P	3975	-742.5	392	S354	5883	807	604	S147	-1961	807	816	G58	-9664	473
181	C2P	4050	-742.5	393	S353	5846	705	605	S146	-1998	705	817	G56	-9566	436
182	C2P	4125	-742.5	394	S352	5809	807	606	S145	-2035	807	818	G54	-9664	399
183	C2P	4200	-742.5	395	S351	5772	705	607	S144	-2072	705	819	G52	-9562	362
184	C2N	4275	-742.5	396	S350	5735	807	608	S143	-2109	807	820	G50	-9664	325
185	C2N	4350	-742.5	397	S349	5698	705	609	S142	-2146	705	821	G48	-9562	288
186	C2N	4425	-742.5	398	S348	5661	807	610	S141	-2183	807	822	G46	-9664	251
187	C2N	4500	-742.5	399	S347	5624	705	611	S140	-2220	705	823	G44	-9562	214
188	VGH	4575	-742.5	400	S346	5587	807	612	S139	-2257	807	824	G42	-9664	177
189	VGH	4650	-742.5	401	S345	5550	705	613	S138	-2294	705	825	G40	-9562	140
190	VGH	4725	-742.5	402	S344	5513	807	614	S137	-2331	807	826	G38	-9664	103
191	VGH	4800	-742.5	403	S343	5476	705	615	S136	-2368	705	827	G36	-9562	66
192	VGH	4875	-742.5	404	S342	5439	807	616	S135	-2405	807	828	G34	-9664	29
193	C3P	4950	-742.5	405	S341	5402	705	617	S134	-2442	705	829	G32	-9562	-8
194	C3P	5025	-742.5	406	S340	5365	807	618	S133	-2479	807	830	G30	-9664	-45
195	C3P	5100	-742.5	407	S339	5328	705	619	S132	-2516	705	831	G28	-9562	-82
196	C3P	5175	-742.5	408	S338	5291	807	620	S131	-2553	807	832	G26	-9664	-119
197	C3N	5250	-742.5	409	S337	5254	705	621	S130	-2590	705	833	G24	-9562	-156
198	C3N	5325	-742.5	410	S336	5217	807	622	S129	-2627	807	834	G22	-9664	-193
199	C3N	5400	-742.5	411	S335	5180	705	623	S128	-2664	705	835	G20	-9562	-230
200	C3N	5475	-742.5	412	S334	5143	807	624	S127	-2701	807	836	G18	-9664	-267
201	VGOFFL	5550	-742.5	413	S333	5106	705	625	S126	-2738	705	837	G16	-9562	-304
202	VGOFFL	5625	-742.5	414	S332	5069	807	626	S125	-2775	807	838	G14	-9664	-341
203	VGOFFL	5700	-742.5	415	S331	5032	705	627	S124	-2812	705	839	G12	-9562	-378
204	VGOFFL	5775	-742.5	416	S330	4995	807	628	S123	-2849	807	840	G10	-9664	-415
205	VGOFFL	5850	-742.5	417	S329	4958	705	629	S122	-2886	705	841	G8	-9562	-452
206	VCI1	5925	-742.5	418	S328	4921	807	630	S121	-2923	807	842	G6	-9664	-489
207	VCI1	6000	-742.5	419	S327	4884	705	631	S120	-2960	705	843	G4	-9562	-526
208	VCI1	6075	-742.5	420	S326	4847	807	632	S119	-2997	807	844	G2	-9664	-563
209	VCIM	6150	-742.5	421	S325	4810	705	633	S118	-3034	705	845	G0	-9562	-600
210	VCIM	6225	-742.5	422	S324	4773	807	634	S117	-3071	807	846	GTESTL	-9664	-637
211	VCIM	6300	-742.5	423	S323	4736	705	635	S116	-3108	705	847	DUMMY	-9562	-681
212	VCHS	6375	-742.5	424	S322	4699	807	636	S115	-3145	807	848	DUMMY	-9664	-732

8 Block Function Description

System Interface

The System Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS3, PS2, PS1 and PS0 pins. Please refer to the pin descriptions on page 5.

a) MPU Parallel 6800-series Interface

The parallel Interface consists of 18 bi-directional data pins (D_{17} – D_0), R/$\overline{W}$, D/$\overline{C}$, E and $\overline{CS}$. R/$\overline{W}$ input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.

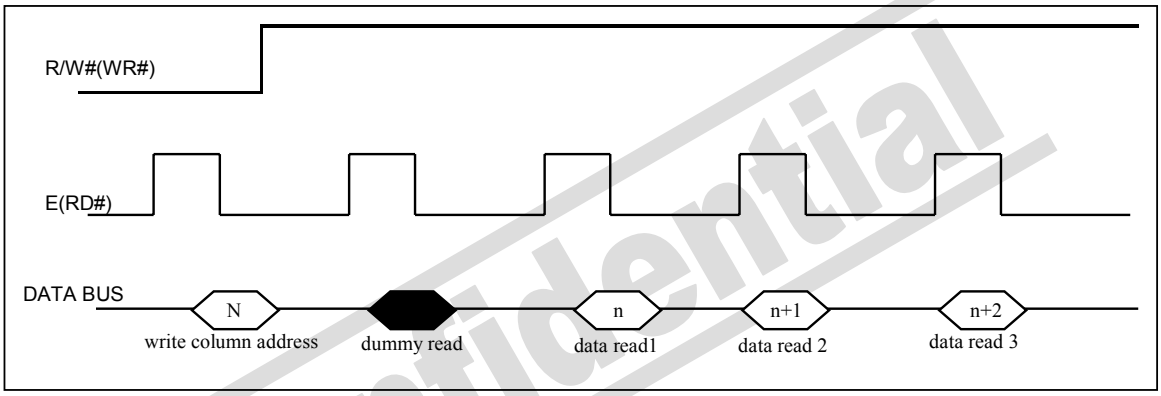


Figure 2 – Read Display Data

b) MPU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins D_{17} – D_0, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$ and $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

c) MPU 4-lines Serial Peripheral Interface

The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$ and $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while D/$\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/$\overline{C}$ bit, D7 to D0 bit. The D/$\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/$\overline{C}$ bit = 1) or the command register (D/$\overline{C}$ bit = 0).

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**MCU Serial Interface**
Data Read	18/16/9/8-bits	18/16/9/8-bits	No
Data Write	18/16/9/8-bits	18/16/9/8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	8-bits

Table 3 - Data bus selection modes

Address Counter (AC)
The address counter (AC) assigns address to the GDDRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.
After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphic Display Data RAM (GDDRAM)
The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 RGB x 176 x 18 / 8 = 52,272 bytes. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command “Data Output/Scan direction” for detail description.
Four pages of display data forms a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command “Set area Scroll” and “Set Scroll Start”.

Gamma/Grayscale Voltage Generator
The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 262,144 possible colors can be displayed when 1 byte = 18 bit. For details, see the gamma-adjusting resistor.

Booster and Regulator Circuit
These two functional blocks generate the voltage of VGH, VGOFFL, VCOM levels and Vlcd0~63 which are necessary for operating a TFT LCD.

Oscillation Circuit (OSC)
This module is an On-Chip low power RC oscillator circuitry. The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.

Data Latches
This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

9 COMMAND TABLE

Table 4 - Command Table

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	Index	0	0	*	*	*	*	*	*	*	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R00h	Oscillation Start	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	OSC EN
	Device code read	1	1	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	0
R01h	Driver output control	0	1	0	0	REV	CAD	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0
R02h	LCD drive AC control	0	1	0	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW6	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Entry mode	0	1	VS Mode	DFM1	DFM0	TRANS	OEDef	WMode	DMode 1	DMode 0	TY1	TY2	ID/1	ID/0	AM	LG2	LG1	LG0
R04h	Compare register (1)	0	1	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0	0	0	CPG5	CPG4	CPG3	CPG2	CPG1	CPG0	0	0
R05h	Compare register (2)	0	1	0	0	0	0	0	0	0	0	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	0	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0
R08h	Reserved																		
R09h	Reserved																		
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0
R0Ch	Reserved																		
R0Dh	Reserved																		
R0Eh	Reserved																		
R10h	Power control (1)	0	1	0	DCY2	DCY1	DCY0	BTH2	BTH1	BTH0	BTL2	BTL1	BTL0	DC1	DC0	AP2	AP1	AP0	SLP
R11h	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	PU1	PU0	VRC2	VRC1	VRC0
R12h	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
R13h	Power control (4)	0	1	0	0	VCOM G	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
R15h	Reserved																		
R16h	Horizontal Porch	0	1	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
R17h	Vertical Porch	0	1	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Ch	Reserved																		
R1Dh	Reserved																		
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R21h	RAM address set	0	1	AD[15:0]															
R22h	RAM data write	0	1	Data[17:0] mapping depends on the interface setting															
	RAM data read	1	1																
R23h	RAM write data mask (1)	0	1	WMR5	WMR4	WMR3	WMR2	WMR1	WMR0	0	0	WMG5	WMG4	WMG3	WMG2	WMG1	WMG0	0	0
R24h	RAM write data mask (2)	0	1	0	0	0	0	0	0	0	0	WMB5	WMB4	WMB3	WMB2	WMB1	WMB0	0	0
R27h	Test Commands	0	1																
R28h	VCOM OTP (1)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R29h	VCOM OTP (2)	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R2A-2Fh	Test Commands	0	1																
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R38h	Reserved																		
R39h	Reserved																		
R3Ah	γ control (9)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
R3Bh	γ control (10)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
R40h	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R41h	Vertical scroll control	0	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
R42h	First display drive position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R43h	Second display drive	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

	position																		
R44h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R45h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Note 1 : * means don't care
Note 2 : Register bits REV, CAD, BGR, TB, RL, CM will override the corresponding hardware pins settings.

10 COMMAND DESCRIPTION

Index / Status / Display control Instruction

Index (IR)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index instruction specifies the RAM control indexes (R00h to RFFh). It sets the register number in the range of 00000000 to 11111111 in binary form. But do not access to Index register and instruction bits which do not have it's own index register.

Device Code Read (R00h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	0	0	0	1	0	0	1	0	1	0	0	0	0	1	1	0

If this register is read forcibly, 1286h is read.

Oscillator (R00h) (POR = 0001h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSCEN

OSCEN: The oscillator will be turned on when OSCEN = 1, off when OSCEN = 0.

Driver Output Control (R01h) (POR = 0383h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	REV	CAD	BGR	SM	TB	RL	MUX7	MUX6	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

REV: Displays all character and graphics display sections with reversal when REV = "1". Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels. Source output level is indicated below.

REV	RGB data	Source Output level	
		VcomH = "L"	VcomH = "H"
0	00000H : 3FFFFH	V63 : V0	V0 : V63
1	00000H : 3FFFFH	V0 : V63	V63 : V0

CAD: Set up based on retention capacitor configuration of the TFT panel.

CAD	Retention capacitor configuration
0	Cs on Common (POR)
1	Cs on Gate

BGR: Selects the <R><G><B> arrangement. When BGR = "0" <R><G><B> color is assigned from S0. When BGR = "1" <B><G><R> color is assigned from S0.

SM: Change scanning order of gate driver. Select the order according to the mounting method.

TB: Selects the output shift direction of the gate driver. When TB = 1, G0 shifts to G175. When TB = 0, G175 shifts to G0.

RL: Selects the output shift direction of the source driver. When RL = "1", S0 shifts to S395 and <R><G><B> color is assigned from S0. When RL = "0", S395 shifts to S0 and <R><G><B> color is assigned from S395. Set RL bit and BGR bit when changing the dot order of R, G and B. RL setting will be ignored when display with RAM (Dmode1-0 = 00).

MUX7-0: Specify number of lines for the LCD driver. Setting exceeds 176 lines (MUX7-0 = 175) will be treated as dummy line of vertical front porch. Refer to "Vertical Porch" (VBH7-0) setting for details.

LCD-Driving-Waveform Control (R02h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD	ENWS	B/C	EOR	WSMD	NW6	NW5	NW4	NW3	NW2	NW1	NW0

FLD: Set display in interlace drive mode to protect from flicker. It splits one frame into 3 fields and drive. When FLD = 1, it is 3 field driving, which also limit VBP = 1 and cannot be used for Cs on gate panel type. That is CAD = 1 & FLD =1 cannot be coexist. When FLD = 0, it is normal driving, either type B or type C depends on B/C.

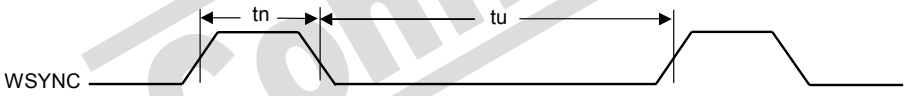
B/C: When B/C = 0, frame inversion of the LCD driving signal is enabled. When B/C = 1, a N-line inversion waveform is generated and alternates in each N lines specified by bits EOR and NW6-0.

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW6-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW6-0 alternate for every set value + 1 lines.

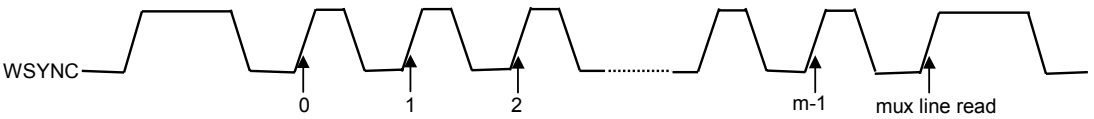
ENWS: When ENWS = 1, it enables WSYNC output pin. Mode1 or Mode2 is selected by WSMD. When ENWS = 0(POR), it disables WSYNC feature, the WSYNC output pin will be high-impedance.

WSMD = 0 is **mode1**, the waveform of WSYNC output will be:



tn is the time when there is No Update of LCD screen from on-chip ram content.
tu is the time when the LCD screen is updating based on on-chip ram content.
e.g. for 176mux, tn = 369us (4 lines), tu =16.25ms (176 lines)

WSMD = 1 is **mode2**, the waveform of WSYNC output will be:



For fast write MCU: MCU should start to write new frame of ram data just after rising edge of long WSYNC pulse and should be finished well before the rising edge of the next long WSYNC pulse.
e.g. 5MHz 8 bit parallel write cycle for 18 bit color depth, or 3MHz 8 bit parallel write cycle for 16 bit color depth.

For slow write MCU (Half the write speed of fast write): MCU should start to write new frame ram data after the rising edge of the first short WSYNC pulse and must be finished within 2 frames time. e.g. 2.5MHz 8 bit parallel write cycle for 18 bit color depth.
* Usually, **mode2** is for slower MCU, while **mode1** is for fast MCU.

Entry Mode (R03h) (POR = 6830h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSMode	DFM1	DFM0	TRANS	OEDef	WMode	DMode1	DMode0	TY1	TY0	ID1	ID0	AM	LG2	LG1	LG0

VSMode: When VSMode = 1 at Dmode1-0 = “00”, the frame frequency will be dependent on VSYNC.

DFM1-0: Set the color display mode.

DFM1	DFM0	Color mode
1	1	65k color (POR)
1	0	262k color

TRANS: When TRANS = 1, transparent display is allowed during Dmode1-0 = “1x”.

OEDef: When OEDef = 1, OE defines the display window.

WMode: When Wmode = 0, write ram from normal data bus.

DMode1-0: SSD1286 allows data display from ram data or from generic input data. When DMode1-0 = “00”, it displays the ram content. When Dmode1-0 = “01”, it displays from generic input data.

Dmode1	Dmode0	Display
0	0	Ram (POR)
0	1	Generic input

TY1-0: In 262k color mode, 16 bit parallel interface, there are three types of methods in writing data into the ram, Type A, B and C are described as below.

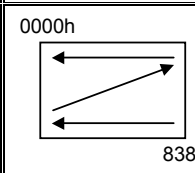
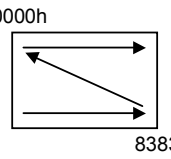
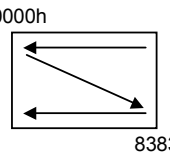
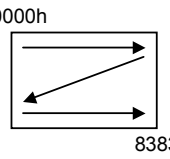
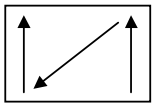
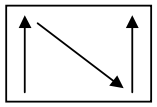
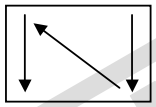
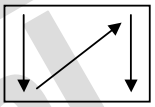
TY1	TY0	Writing mode
0	0	Type A
0	1	Type B
1	0	Type C

			Hardware pins																
Interface	Color mode	Cycle	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 bit	262k Type A	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type B	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	G4	B3	B2	B1	B0	x	x	
	262k Type C	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	G4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	

Remark : x Don't care bits
Not connected pins

ID1-0: The address counter is automatically incremented by 1, after data are written to the GDDRAM when ID1-0 = “1”. The address counter is automatically decremented by 1, after data are written to the GDDRAM when ID1-0 = “0”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data are written to the GDDRAM is set with AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the GDDRAM. When AM = “0”, the address counter is updated in the horizontal direction. When AM = “1”, the address counter is updated in the vertical direction. When window addresses are selected, data are written to the GDDRAM area specified by the window addresses in the manner specified with ID1-0 and AM bits.

	I/D1-0="00” Horizontal: decrement Vertical: decrement	I/D1-0="01” Horizontal: increment Vertical: decrement	I/D1-0="10” Horizontal: decrement Vertical: increment	I/D1-0="11” Horizontal: increment Vertical: increment
AM="0” Horizontal				
AM="1” Vertical				

LG2–0: Write data to the GDDRAM after comparing the write data written to the GDDRAM by the microcomputer with the values in the compare registers (CPR5-0, CPG5-0, CPB5-0) and performing a logical and arithmetic operation on them.

Compare register (R04h – R05h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	CPR5	CPR4	CPR3	CPR2	CPR1	CPR0	0	0	CPG5	CPG4	CPG3	CPG2	CPG1	CPG0	0	0
W	1	0	0	0	0	0	0	0	0	CPB5	CPB4	CPB3	CPB2	CPB1	CPB0	0	0

CPR5-0, CPG5-0, CPB5–0: Set the value for the compare register, of which the data read out from the GDDRAM or data written to the GDDRAM by the microcomputer are compared. This function is not available in the external display interface mode. In the external display mode, make sure LG2-0 = "000". CPR5-0 compares the pins RR5-0, CPG5-0 compares the pins GG5-0, and CPB5-0 compares the pins BB5-0. Refer to Section 14 Interface Mapping for writing methods in RGB data.

Display Control (R07h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CM	0	D1	D0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven.

VLE2–1: When VLE1 = 1 or VLE2 = 1, a vertical scroll is performed in the 1st screen by taking data VL17-0 in R41h register. When VLE2 = 1 and VLE1 = 1, a vertical scroll is performed in the 1st and 2nd screen by VL17-0 and VL27-0 respectively.

SPT: When SPT = "1", the 2-division LCD drive is performed.

CM: When CM = 1, 8-color mode is selected.

GON: Gate off level becomes VGH when GON = "0".

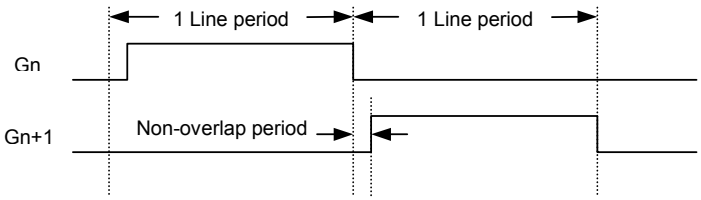
D1–0: Display is on when D1 = "1" and off when D1 = "0". When off, the display data remains in the GDDRAM, and can be displayed instantly by setting D1 = "1". When D1= "0", the display is off with all of the source outputs set to the GND level. Because of this, the driver can control the charging current for the LCD with AC driving. When D1–0 = "01", the internal display is performed although the display is off. When D1-0 = "00", the internal display operation halts and the display is off. Control the display on/off while control GON and DTE.

Frame Cycle Control (R0Bh) (POR = 540Ah)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	SDIV	SRTN	RTN3	RTN2	RTN1	RTN0

NO1-0: Sets amount of non-overlap of the gate output.

NO1	NO0	Amount of non-overlap
0	0	0 clock cycle
0	1	4 clock cycle
1	0	6 clock cycle
1	1	8 clock cycle

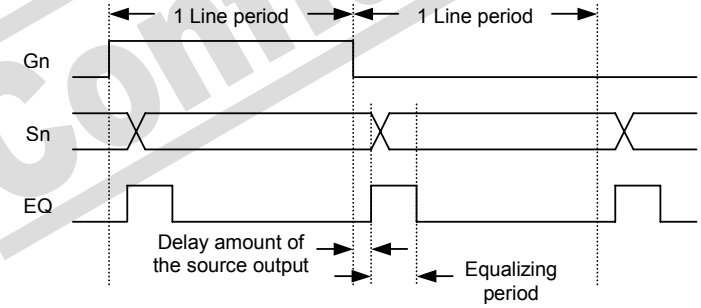


SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

SDT1	SDT0	Delay amount of the source output
0	0	1 clock cycle
0	1	2 clock cycle
1	0	3 clock cycle
1	1	4 clock cycle

EQ1-0: Sets the equalizing period.

EQ1	EQ0	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle



DIV1-0: Set the division ratio of clocks for internal operation. Internal operations are driven by clocks which frequency is divided according to the DIV1-0 setting.

DIV1	DIV0	Division Ratio
0	0	1
0	1	2
1	0	4
1	1	8

* fosc = internal oscillator frequency, ~500kHz

SDIV: When SDIV = 1, DIV1-0 value will be count. When SDIV = 0, DIV1-0 value will be auto determined.

SRTN: When SRTN =1, RTN3-0 value will be count. When SRTN = 0, RTN3-0 value will be auto determined.

RTN3-0: Set the no. of clocks in each line. The total number will be the decimal value of RTN3-0 plus 16. e.g. if RTN3-0 = “1010h”, the total number of clocks in each line = 10 +16 = 26 clocks.

Power control 1 (R10h) (POR = 2FC1h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	DCY2	DCY1	DCY0	BTH2	BTH1	BTH0	BTL2	BTL1	BTL0	DC1	DC0	AP2	AP1	AP0	SLP

DCY2-0: Set the step-up cycle of the step-up circuit for high voltage output. When the cycle accelerates, the driving ability of the step-up circuit increases, but its current consumption also increases. Adjust the cycle by taking into account the display quality and the power consumption.

DCY2	DCY1	DCY0	Step-up cycle
0	0	0	Fline x 8
0	0	1	Fline x 4
0	1	0	Fline x 2 (POR if 262k mode)
0	1	1	Fline x 1
1	0	0	fosc / 4
1	0	1	fosc / 8
1	1	0	fosc / 16 (POR if 8 color mode)
1	1	1	fosc / 32

*fosc = internal oscillator frequency
*Fline = line frequency

BTH2-0: Control the step-up factor of the step-up circuit on VGH. Adjust the step-up factor according to the power-supply voltage to be used.

BTH2	BTH1	BTH0	VGH output
0	0	0	8V
0	0	1	9V
0	1	0	10V
0	1	1	11V
1	0	0	12V
1	0	1	13V
1	1	0	14V
1	1	1	15V

BTL2-0: Control the step-up factor of the step-up circuit on VgoffL. Adjust the step-up factor according to the power-supply voltage to be used.

BTL2	BTL1	BTL0	VgoffL output
0	0	0	-{(VGH – Vref) x 0.70 – Vref}
0	0	1	-{(VGH – Vref) x 0.75 – Vref}
0	1	0	-{(VGH – Vref) x 0.80 – Vref}
0	1	1	-{(VGH – Vref) x 0.85 – Vref}
1	0	0	-{(VGH – Vref) x 0.90 – Vref}
1	0	1	-{(VGH – Vref) x 0.95 – Vref}
1	1	0	-{(VGH – Vref) x 1.00 – Vref}
1	1	1	Unregulated

*Vref = internal voltage reference = 1.2V

DC1-0: Set the step-up cycle of the step-up circuit for VCIX2. When the cycle accelerates, the driving ability of the step-up circuit increases, but its current consumption also increases. Adjust the cycle taking into account the display quality and power consumption.

DC1	DC0	Step-up cycle
0	0	fosc (POR)
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

* fosc = internal oscillator frequency

AP2-0: Adjust the amount of current form the stable-current source in the internal operational amplifier circuit. When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase. Adjust the current by taking into account the power consumption. While there is no display, such as the system is in a sleep mode, AP2-0 can be set to (0,0,0) and shutting down the operational amplifier can reduce the power consumption.

AP2	AP1	AP0	Op-amp power
0	0	0	Least (POR)
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Reserved
1	1	1	Reserved

SLP: When SLP = 1, the driver enters into the sleep mode. In the sleep mode, the internal display operations are halted except the R-C oscillator to reduce current consumption. Only the power control instructions (R10h – R13h) are executed during the sleep mode. No change in the GDDRAM data or instructions during the sleep mode is made, although it is retained.

Power Control 2 (R11h) (POR = 001Ch)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PU1	PU0	VRC2	VRC1	VRC0

PU1-0: Set the step up multiplying ratio of VGH from VCI. This determines the maximum level of VGH.

PU1	PU0	VGH/VCI ratio
0	0	x3
0	1	X4
1	0	X5
1	1	X6 (POR)

VRC2-0: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	VCIX2 voltage
0	0	0	5.1V
0	0	1	5.2V
0	1	0	5.3V
0	1	1	5.4V
1	0	0	5.5V (POR)
1	0	1	5.6V
1	1	0	5.7V
1	1	1	5.8V

Power Control 3 (R12h) (POR = 0608h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	1	1	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0

VRH3-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 1.33 to 2.85 times the voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	VLCD63 Voltage
0	0	0	0	Vref x 1.330
0	0	0	1	Vref x 1.450
0	0	1	0	Vref x 1.550
0	0	1	1	Vref x 1.650
0	1	0	0	Vref x 1.750
0	1	0	1	Vref x 1.800
0	1	1	0	Vref x 1.850
0	1	1	1	Stopped
1	0	0	0	Vref x 1.900 (POR)
1	0	0	1	Vref x 2.175
1	0	1	0	Vref x 2.325
1	0	1	1	Vref x 2.475
1	1	0	0	Vref x 2.625
1	1	0	1	Vref x 2.700
1	1	1	0	Vref x 2.775
1	1	1	1	Stopped

*Vref is the internal reference voltage equals to 2.0V.

Power Control 4 (R13h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0

VcomG: When VcomG = "1", it is possible to set output voltage of VcomL to any level, and the instruction (VDV4-0) becomes available. When VcomG = "0", VcomL output is fixed to Hi-z level, VCIM output for VcomL power supply stops, and the instruction (VDV4-0) becomes unavailable. Set VcomG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-0: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify 0.6 to 1.23 times the VLCD63 voltage. When VcomG = "0", the settings become invalid. External voltage at VcomR is referenced when VDH = "01111".

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
0	0	0	1	0	VLCD63 x 0.66
		: : :			: Step = 0.03 :
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reference from external variable resistor
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		: : :			: Step = 0.03 :
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

Note: Vcom amplitude < 5V

Horizontal Porch (R16h) (POR = 8302h)

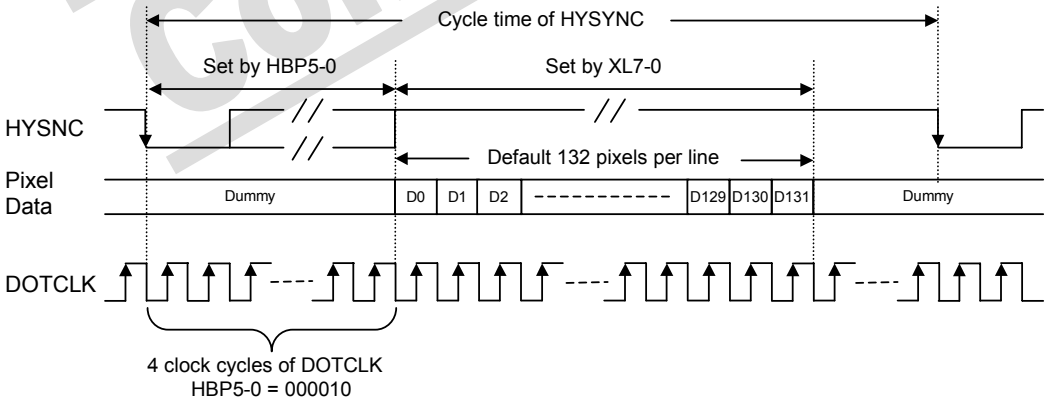
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

XL7-0: Set the number of valid pixel per line.

XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	No. of pixel per line
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
:	:	:	:	:	:	:	:	: Step = 1 :
1	0	0	0	0	0	1	0	131
1	0	0	0	0	0	1	1	132 (POR)
1	0	0	0	0	1	*	*	Reserved
1	1	*	*	*	*	*	*	Reserved

HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data. The pixel data exceed the range set by XL7-0 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	No. of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4 (POR)
0	0	0	0	1	1	5
0	0	0	1	0	0	6
0	0	0	1	0	1	7
0	0	0	1	1	0	8
0	0	0	1	1	1	9
0	0	1	0	0	0	10
:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65



Vertical Porch (R17h) (POR = 0402h)

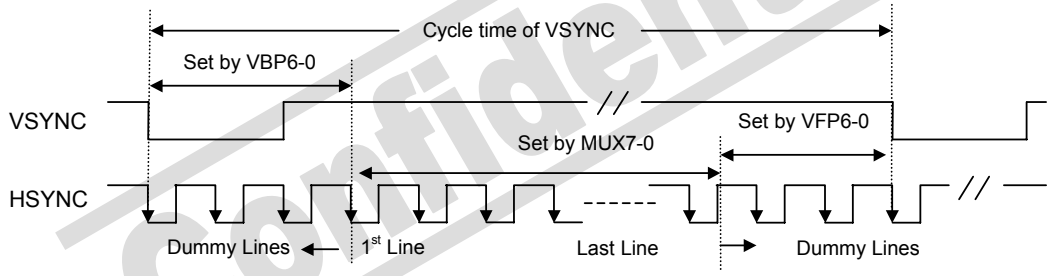
R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

VFP6-0: Set the delay period from the last valid line to the falling edge of VSYNC of the next frame. The line data within this delay period will be treated as dummy line.

VFP6	VFP5	VFP4	VFP3	VFP2	VFP1	VFP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
0	0	0	0	0	1	1	4
0	0	0	0	1	0	0	5 (POR)
:	:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128

VBP6-0: Set the delay period from falling edge of VSYNC to first valid line. The line data within this delay period will be treated as dummy line.

VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	No. of clock cycle of HSYNC
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3 (POR)
0	0	0	0	0	1	1	4
0	0	0	0	1	0	0	5
:	:	:	:	:	:	:	: Step = 1 :
1	1	1	1	1	1	0	127
1	1	1	1	1	1	1	128



Power Control 5 (R1Eh) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0

nOTP: nOTP equals to "0" after power on reset and VcomH voltage equals to programmed OTP value. When nOTP set to "1", setting of VCM5-0 becomes valid and voltage of VcomH can be adjusted.

VCM5-0: Set the VcomH voltage if nOTP = "1". These bits amplify the VcomH voltage 0.35 to 0.99 times the VLCD63 voltage. Default value is "101000" when power on reset.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VcomH
0	0	0	0	0	0	VLCD63 x 0.35
0	0	0	0	0	1	VLCD63 x 0.36
:	:	:	:	:	:	: Step = 0.01 :
1	1	1	1	1	0	VLCD63 x 0.98
1	1	1	1	1	1	VLCD63 x 0.99

Note: 2V < VcomH < VCIx2

RAM address set (R21h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD15–0: Make initial settings for the GDDRAM address in the address counter (AC). After GRAM data are written, the address counter is automatically updated according to the settings with AM, I/D bits and setting for a new GDDRAM address is not required in the address counter. Therefore, data are written consecutively without setting an address. The address counter is not automatically updated when data are read out from the GDDRAM.

GDDRAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses.

Write Data to GRAM (R22h)

R/W	DC	D[17:0]
W	1	WD[17:0] mapping depends on the interface setting

WD17–0: Transforms all the GDDRAM data into 18-bit, and writes the data. Format for transforming data into 18-bit depends on the interface used. SSD1286 selects the grayscale level according to the GDDRAM data. After writing data to GDDRAM, address is automatically updated according to AM bit and ID bit. Access to GDDRAM during stand-by mode is not available.

Read Data from GRAM (R22h)

R/W	DC	D[17:0]
R	1	RD[17:0] mapping depends on the interface setting

RD17–0: Read 18-bit data from the GDDRAM. When the data is read to the microcomputer, the first-word read immediately after the GDDRAM address setting is latched from the GDDRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed, only one read can be processed since the latched data in the first word is used.

RAM write data mask (R23h – R24h) (POR = 0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WMR5	WMR4	WMR3	WMR2	WMR1	WMR0	0	0	WMG5	WMG4	WMG3	WMG2	WMG1	WMG0	0	0
W	1	0	0	0	0	0	0	0	0	WMB5	WMB4	WMB3	WMB2	WMB1	WMB0	0	0

WMR5-0, WMG5-0, WMB5-0: In writing to the GDDRAM, these bits write-mask the data to be written to the GDDRAM by a bit unit. For example, if WMR5 = 1, the WMR5 write-mask is enabled and data RR5 will be masked and not write into the GDDRAM. WMR5-0 mask pins RR5-0, WMG5-0 mask pins GG5-0, and WMB5-0 mask pins BB5-0. For writing GDDRAM methods, refer to Section 14 Interface Mapping".

Vcom OTP (R28h – R29h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
W	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

When OTP is access, theses registers must be set accordantly.

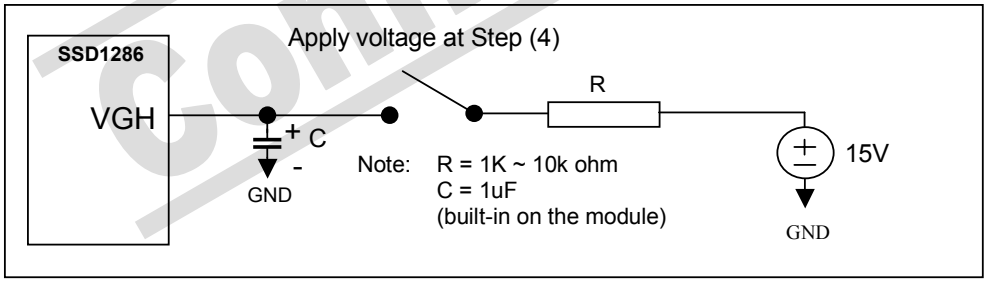
OTP programming sequence

Step	Operation
1	Power up the module at VCI = 2.7V, VDD = VDDIO = 1.8V. Turn on the display as normal to 65k/262k color mode (displaying a test pattern if any).
2	Set nOTP to "1" (R1Eh) and optimizes VcomH by adjusting VCM[5:0] (R1Eh).
3	Power down the whole module.
4	Connect a supply to the module at VCI = 3.0V, VDD = VDDIO = 1.8V, VGH = 15V
5	Write below commands for OTP initialization and wait for 200ms for activate the OTP :

Index	Value
R00h	0x0001
R28h	0x0006
R29h	0x80C0
R10h	0x2FC0
R07h	0x0033
R28h	0x0A81

6	Write the optimized value found in Step 2 to VCM[5:0] (R1Eh) and set nOTP to "1".
7	Fire the OTP by write HEX code "000Ah" to register R28h.
8	Wait at least 3 seconds.
9	OTP complete. Power down the whole module and remove 15V supply.

Note: nOTP must set to "0" to activate the OTP effect.



Gamma Control (R30h to R3Bh)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
W	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

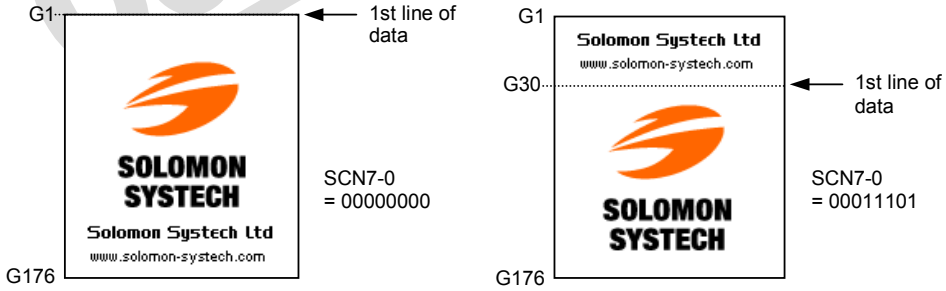
PRN12-00: Gradient adjustment register for the negative polarity output

VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output. (For details, see the Chapter 11 Gamma Adjustment Function).

Gate Scan Position (R40h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN7-0: Set the scanning starting position of the gate driver. The valid range is from 0 to 131.



Vertical Scroll Control (R41h) (POR =0000h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10

VL27-0: Specify scroll length at the scroll display for vertical smooth scrolling at 2nd screen. The display-start raster-row (VL27-0) is valid when VLE1 = "1" and VLE2 = "1".

VL17-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 132nd can be scrolled for the number of the raster-row. After 132nd raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL17-0) is valid when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE2-1 = "00".

1st Screen driving position (R42h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the set value + 1 gate driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SS17–10 = "07"H and SE17–10 = "10"H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ 83H.

2nd Screen driving position (R43h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the set value + 1 gate driver. The second screen is driven when SPT = "1".

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the set value + 1 gate driver. For instance, when SPT = "1", SS27–20 = "20"H, and SE27–20 = "2F"H are set, the LCD driving is performed from G33 to G48. Ensure that SS17–10 ≤ SE17–10 ; SS27–20 ≤ SE27–20 ≤ 83H.

Horizontal RAM address position (R44h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0

HSA7-0/HEA7-0: Specify the start/end positions of the window address in the horizontal direction by an address unit. Data are written to the GDDRAM within the area determined by the addresses specified by HEA7-0 and HSA7-0. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "83"h.

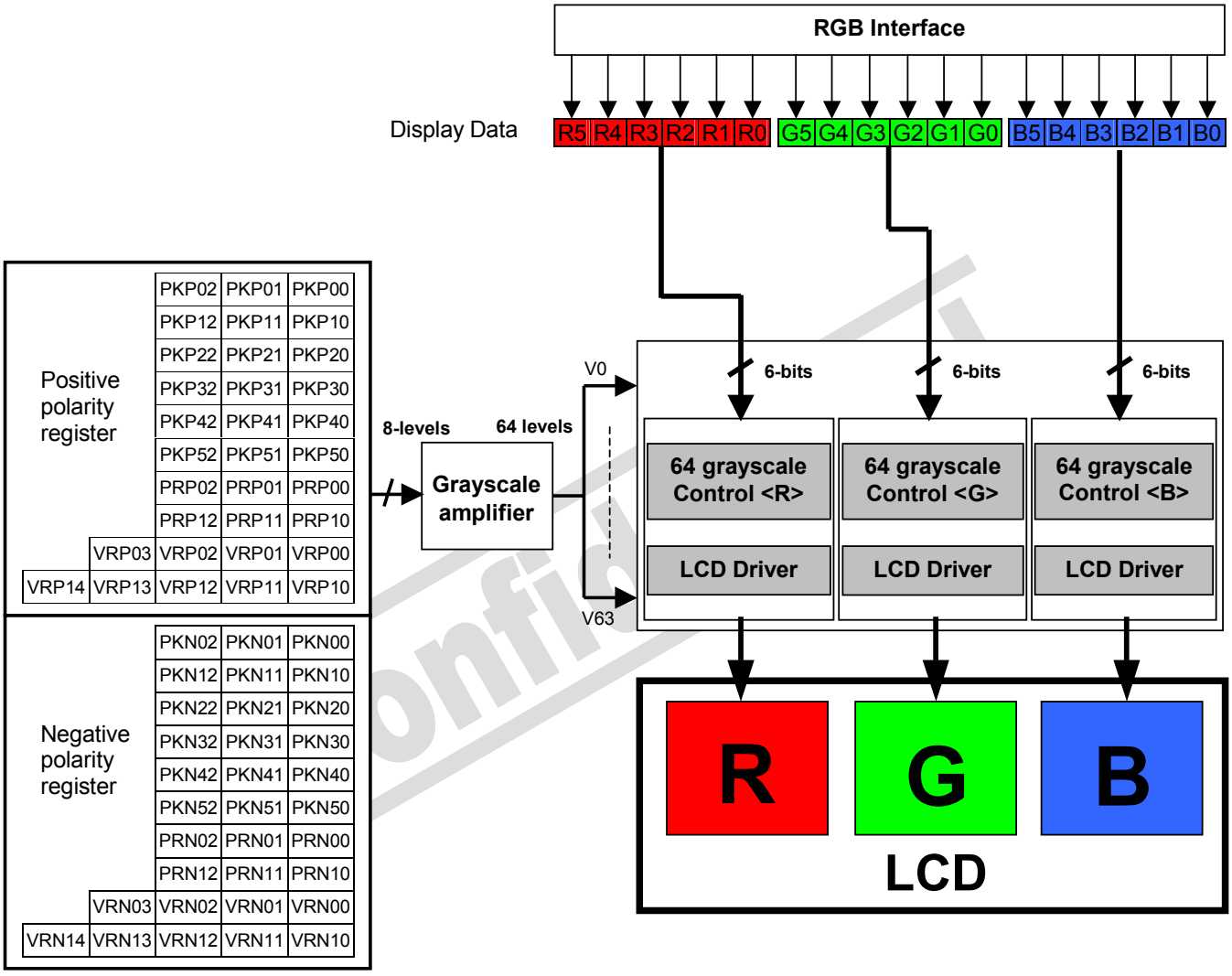
Vertical RAM address position (R45h) (POR = 8300h)

R/W	DC	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

VSA7-0/VEA7-0: Specify the start/end positions of the window address in the vertical direction by an address unit. Data are written to the GRAM within the area determined by the addresses specified by VEA7-0 and VSA7-0. These addresses must be set before the RAM write. In setting these bits, make sure that "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "83"h.

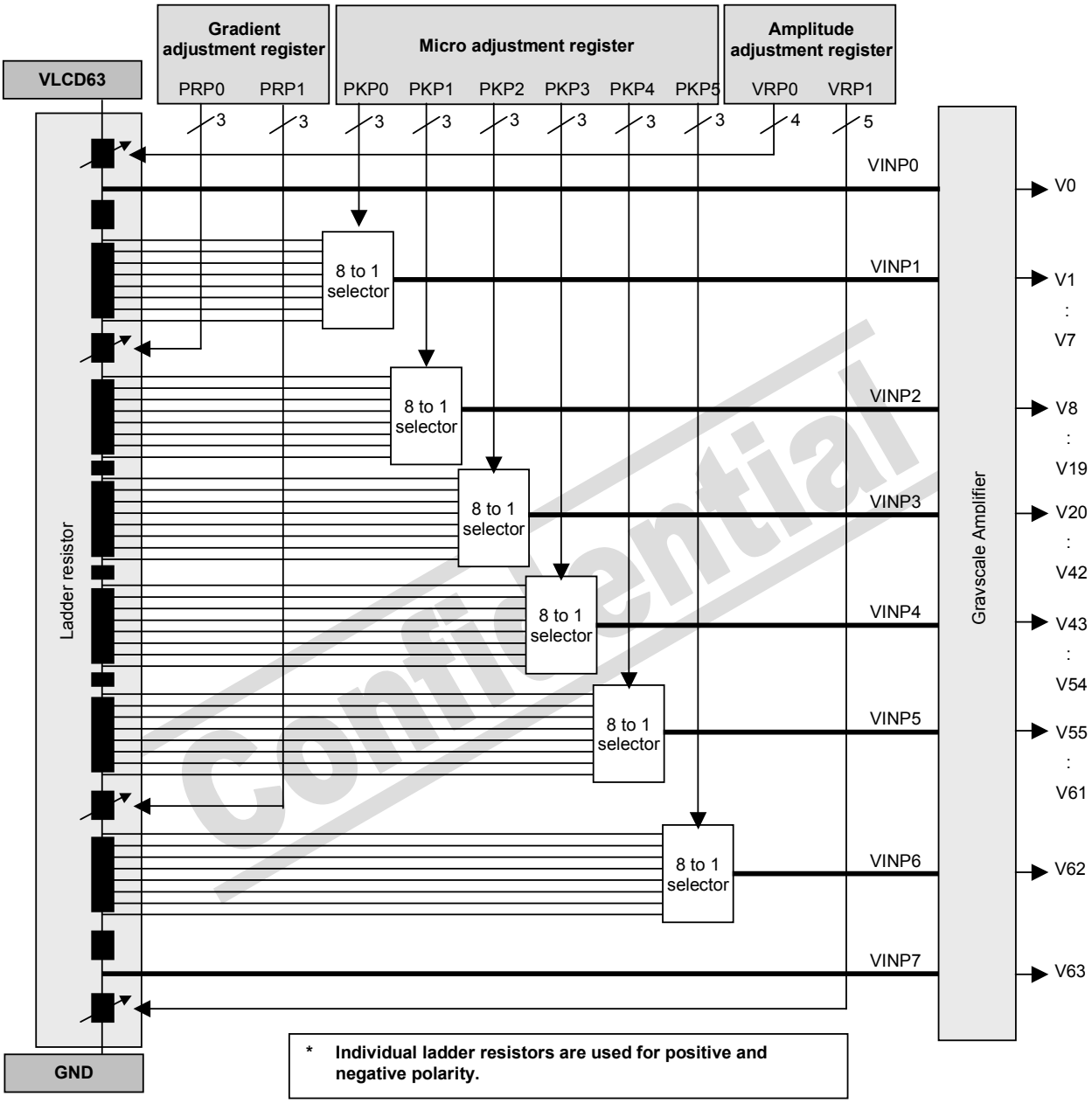
11 Gamma Adjustment Function

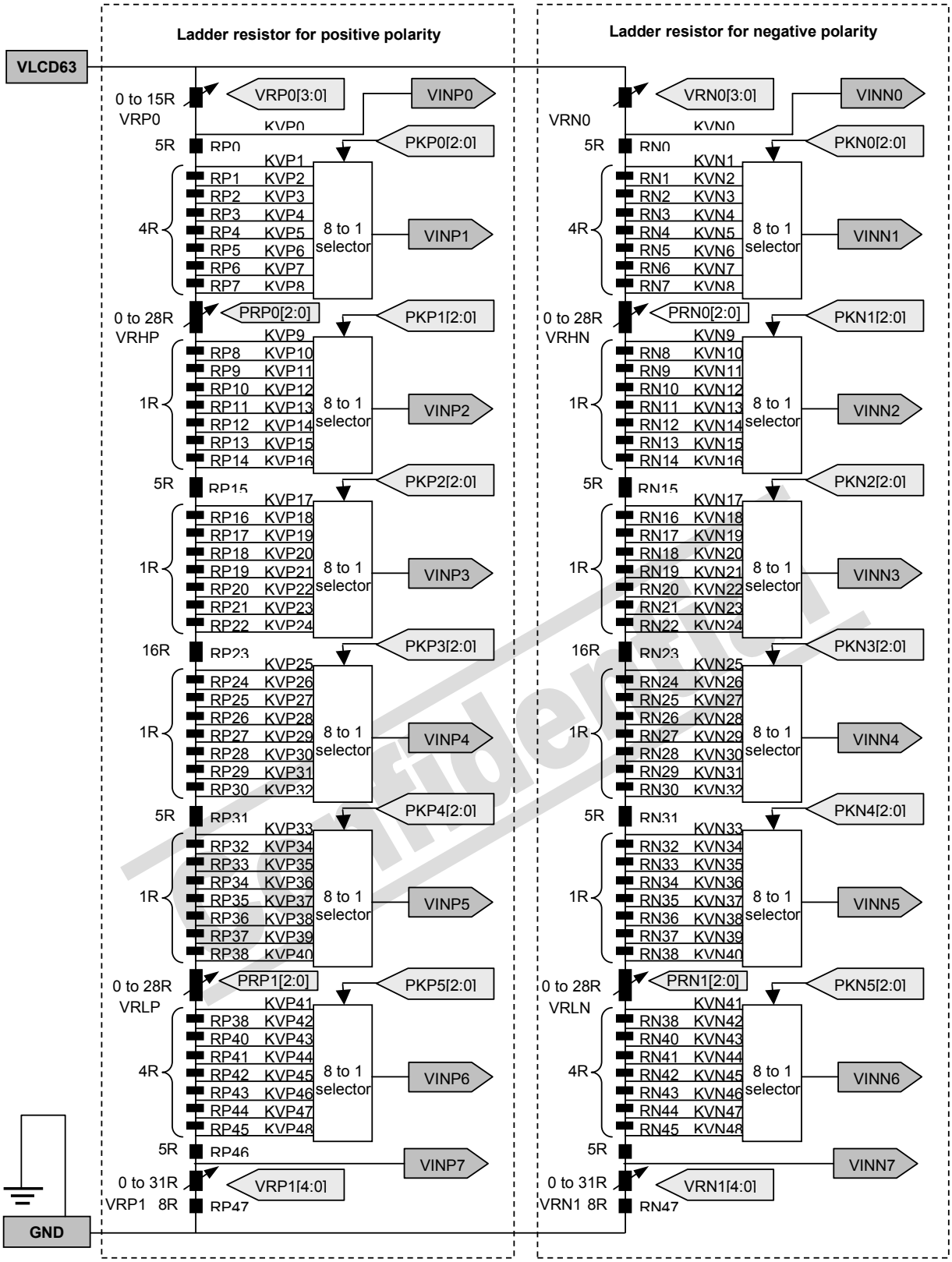
The SSD1286 incorporates gamma adjustment function for the 262,144-color display. Gamma adjustment is implemented by deciding the 8-grayscale levels with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.



11.1 Structure of Grayscale Amplifier

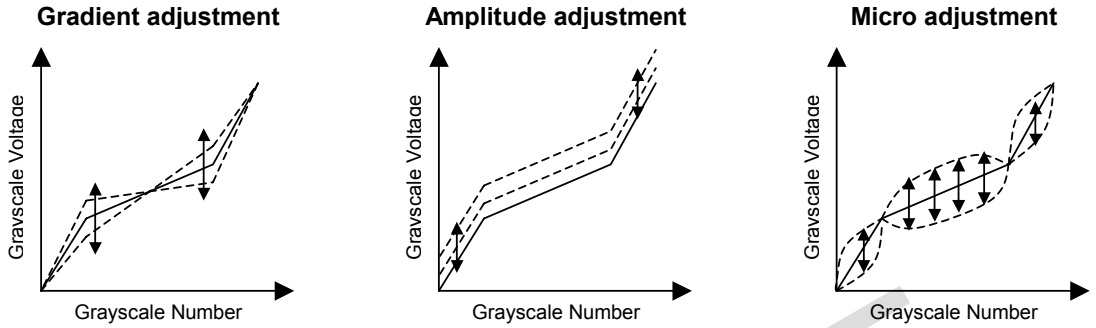
Below figure indicates the structure of the grayscale amplifier. It determines 8 levels (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V63.




Ladder resistor for positive polarity
Ladder resistor for negative polarity
VLCD63
GND
0 to 15R
VRP0
5R
4R
1R
16R
0 to 28R
VRHP
VRLP
0 to 31R
VRP1
8R
VRP0[3:0]
PRP0[2:0]
PRP1[2:0]
VRP1[4:0]
VINP0
VINP1
VINP2
VINP3
VINP4
VINP5
VINP6
VINP7
PKP0[2:0]
PKP1[2:0]
PKP2[2:0]
PKP3[2:0]
PKP4[2:0]
PKP5[2:0]
8 to 1 selector
VRN0
VRHN
VRLN
VRN1
VRN0[3:0]
PRN0[2:0]
PRN1[2:0]
VRN1[4:0]
VINN0
VINN1
VINN2
VINN3
VINN4
VINN5
VINN6
VINN7
PKN0[2:0]
PKN1[2:0]
PKN2[2:0]
PKN3[2:0]
PKN4[2:0]
PKN5[2:0]

11.2 Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are three types of register groups to adjust gradient, amplitude, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.



11.2.1 Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistors in the middle of the ladder resistor by registers (PRP(N)0 / PRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

11.2.2 Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistors in the boundary of the ladder resistor by registers (VRP(N)0 / VRP(N)1) for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

11.2.3 Micro adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-level reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

11.3 Ladder Resistor / 8 to 1 selector

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors.

Variable Resistor

There are 3 types of the variable resistors that are for the gradient and amplitude adjustment. The resistance is set by the resistor (PRP(N)0 / PRP(N)1) and (VRP(N)0 / VRP(N)1) as below.

PRP(N)[0:1]	Resistance
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

VRP(N)0	Resistance
0000	0R
0001	1R
0010	2R
: Step = R :	
1110	14R
1111	15R

VRP(N)1	Resistance
00000	0R
00001	1R
00010	2R
: Step = 1R :	
11110	30R
11111	31R

8 to 1 selecter

In the 8 to 1 selector, a reference voltage VIN can be selected from the levels which are generated by the ladder resistors. There are six types of reference voltage (VIN1 to VIN6) and totally 48 divided voltages can be selected in one ladder resistor. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Postive polarity							Negative polarity						
Registor	Selected voltage						Registor	Selected voltage					
PKP[2:0]	VINP1	VINP2	VINP3	VINP4	VINP5	VINP6	PKN[2:0]	VINN1	VINN2	VINN3	VINN4	VINN5	VINN6
000	KVP1	KVP9	KVP17	KVP25	KVP33	KVP41	000	KVN1	KVN9	KVN17	KVN25	KVN33	KVN41
001	KVP2	KVP10	KVP18	KVP26	KVP34	KVP42	001	KVN2	KVN10	KVN18	KVN26	KVN34	KVN42
010	KVP3	KVP11	KVP19	KVP27	KVP35	KVP43	010	KVN3	KVN11	KVN19	KVN27	KVN35	KVN43
011	KVP4	KVP12	KVP20	KVP28	KVP36	KVP44	011	KVN4	KVN12	KVN20	KVN28	KVN36	KVN44
100	KVP5	KVP13	KVP21	KVP29	KVP37	KVP45	100	KVN5	KVN13	KVN21	KVN29	KVN37	KVN45
101	KVP6	KVP14	KVP22	KVP30	KVP38	KVP46	101	KVN6	KVN14	KVN22	KVN30	KVN38	KVN46
110	KVP7	KVP15	KVP23	KVP31	KVP39	KVP47	110	KVN7	KVN15	KVN23	KVN31	KVN39	KVN47
111	KVP8	KVP16	KVP24	KVP32	KVP40	KVP48	111	KVN8	KVN16	KVN24	KVN32	KVN40	KVN48

Grayscale voltage	Formula	Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP(N)0	V22	V43+(V20-V43)*(21/23)	V44	V55+(V43-V55)*(22/24)
V1	VINP(N)1	V23	V43+(V20-V43)*(20/23)	V45	V55+(V43-V55)*(20/24)
V2	V8+(V1-V8)*(30/48)	V24	V43+(V20-V43)*(19/23)	V46	V55+(V43-V55)*(18/24)
V3	V8+(V1-V8)*(23/48)	V25	V43+(V20-V43)*(18/23)	V47	V55+(V43-V55)*(16/24)
V4	V8+(V1-V8)*(16/48)	V26	V43+(V20-V43)*(17/23)	V48	V55+(V43-V55)*(14/24)
V5	V8+(V1-V8)*(12/48)	V27	V43+(V20-V43)*(16/23)	V49	V55+(V43-V55)*(12/24)
V6	V8+(V1-V8)*(8/48)	V28	V43+(V20-V43)*(15/23)	V50	V55+(V43-V55)*(10/24)
V7	V8+(V1-V8)*(4/48)	V29	V43+(V20-V43)*(14/23)	V51	V55+(V43-V55)*(8/24)
V8	VINP(N)2	V30	V43+(V20-V43)*(13/23)	V52	V55+(V43-V55)*(6/24)
V9	V20+(V8-V20)*(22/24)	V31	V43+(V20-V43)*(12/23)	V53	V55+(V43-V55)*(4/24)
V10	V20+(V8-V20)*(20/24)	V32	V43+(V20-V43)*(11/23)	V54	V55+(V43-V55)*(2/24)
V11	V20+(V8-V20)*(18/24)	V33	V43+(V20-V43)*(10/23)	V55	VINP(N)5
V12	V20+(V8-V20)*(16/24)	V34	V43+(V20-V43)*(9/23)	V56	V62+(V55-V62)*(44/48)
V13	V20+(V8-V20)*(14/24)	V35	V43+(V20-V43)*(8/23)	V57	V62+(V55-V62)*(40/48)
V14	V20+(V8-V20)*(12/24)	V36	V43+(V20-V43)*(7/23)	V58	V62+(V55-V62)*(36/48)
V15	V20+(V8-V20)*(10/24)	V37	V43+(V20-V43)*(6/23)	V59	V62+(V55-V62)*(32/48)
V16	V20+(V8-V20)*(8/24)	V38	V43+(V20-V43)*(5/23)	V60	V62+(V55-V62)*(25/48)
V17	V20+(V8-V20)*(6/24)	V39	V43+(V20-V43)*(4/23)	V61	V62+(V55-V62)*(18/48)
V18	V20+(V8-V20)*(4/24)	V40	V43+(V20-V43)*(3/23)	V62	VINP(N)6
V19	V20+(V8-V20)*(2/24)	V41	V43+(V20-V43)*(2/23)	V63	VINP(N)7
V20	VINP(N)3	V42	V43+(V20-V43)*(1/23)		
V21	V43+(V20-V43)*(22/23)	V43	VINP(N)4		

Reference voltage of positive polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVP0	VLCD63 - ΔV x VRP0 / SUMRP	--	VINP0
KVP1	VLCD63 - ΔV x (VRP0 + 5R) / SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	VLCD63 - ΔV x (VRP0 + 9R) / SUMRP	PKP0[2:0] = “001”	
KVP3	VLCD63 - ΔV x (VRP0 + 13R) / SUMRP	PKP0[2:0] = “010”	
KVP4	VLCD63 - ΔV x (VRP0 + 17R) / SUMRP	PKP0[2:0] = “011”	
KVP5	VLCD63 - ΔV x (VRP0 + 21R) / SUMRP	PKP0[2:0] = “100”	
KVP6	VLCD63 - ΔV x (VRP0 + 25R) / SUMRP	PKP0[2:0] = “101”	
KVP7	VLCD63 - ΔV x (VRP0 + 29R) / SUMRP	PKP0[2:0] = “110”	
KVP8	VLCD63 - ΔV x (VRP0 + 33R) / SUMRP	PKP0[2:0] = “111”	
KVP9	VLCD63 - ΔV x (VRP0 + 33R + VRHP) / SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	VLCD63 - ΔV x (VRP0 + 34R + VRHP) / SUMRP	PKP1[2:0] = “001”	
KVP11	VLCD63 - ΔV x (VRP0 + 35R + VRHP) / SUMRP	PKP1[2:0] = “010”	
KVP12	VLCD63 - ΔV x (VRP0 + 36R + VRHP) / SUMRP	PKP1[2:0] = “011”	
KVP13	VLCD63 - ΔV x (VRP0 + 37R + VRHP) / SUMRP	PKP1[2:0] = “100”	
KVP14	VLCD63 - ΔV x (VRP0 + 38R + VRHP) / SUMRP	PKP1[2:0] = “101”	
KVP15	VLCD63 - ΔV x (VRP0 + 39R + VRHP) / SUMRP	PKP1[2:0] = “110”	
KVP16	VLCD63 - ΔV x (VRP0 + 40R + VRHP) / SUMRP	PKP1[2:0] = “111”	
KVP17	VLCD63 - ΔV x (VRP0 + 45R + VRHP) / SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	VLCD63 - ΔV x (VRP0 + 46R + VRHP) / SUMRP	PKP2[2:0] = “001”	
KVP19	VLCD63 - ΔV x (VRP0 + 47R + VRHP) / SUMRP	PKP2[2:0] = “010”	
KVP20	VLCD63 - ΔV x (VRP0 + 48R + VRHP) / SUMRP	PKP2[2:0] = “011”	
KVP21	VLCD63 - ΔV x (VRP0 + 49R + VRHP) / SUMRP	PKP2[2:0] = “100”	
KVP22	VLCD63 - ΔV x (VRP0 + 50R + VRHP) / SUMRP	PKP2[2:0] = “101”	
KVP23	VLCD63 - ΔV x (VRP0 + 51R + VRHP) / SUMRP	PKP2[2:0] = “110”	
KVP24	VLCD63 - ΔV x (VRP0 + 52R + VRHP) / SUMRP	PKP2[2:0] = “111”	
KVP25	VLCD63 - ΔV x (VRP0 + 68R + VRHP) / SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	VLCD63 - ΔV x (VRP0 + 69R + VRHP) / SUMRP	PKP3[2:0] = “001”	
KVP27	VLCD63 - ΔV x (VRP0 + 70R + VRHP) / SUMRP	PKP3[2:0] = “010”	
KVP28	VLCD63 - ΔV x (VRP0 + 71R + VRHP) / SUMRP	PKP3[2:0] = “011”	
KVP29	VLCD63 - ΔV x (VRP0 + 72R + VRHP) / SUMRP	PKP3[2:0] = “100”	
KVP30	VLCD63 - ΔV x (VRP0 + 73R + VRHP) / SUMRP	PKP3[2:0] = “101”	
KVP31	VLCD63 - ΔV x (VRP0 + 74R + VRHP) / SUMRP	PKP3[2:0] = “110”	
KVP32	VLCD63 - ΔV x (VRP0 + 75R + VRHP) / SUMRP	PKP3[2:0] = “111”	
KVP33	VLCD63 - ΔV x (VRP0 + 80R + VRHP) / SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	VLCD63 - ΔV x (VRP0 + 81R + VRHP) / SUMRP	PKP4[2:0] = “001”	
KVP35	VLCD63 - ΔV x (VRP0 + 82R + VRHP) / SUMRP	PKP4[2:0] = “010”	
KVP36	VLCD63 - ΔV x (VRP0 + 83R + VRHP) / SUMRP	PKP4[2:0] = “011”	
KVP37	VLCD63 - ΔV x (VRP0 + 84R + VRHP) / SUMRP	PKP4[2:0] = “100”	
KVP38	VLCD63 - ΔV x (VRP0 + 85R + VRHP) / SUMRP	PKP4[2:0] = “101”	
KVP39	VLCD63 - ΔV x (VRP0 + 86R + VRHP) / SUMRP	PKP4[2:0] = “110”	
KVP40	VLCD63 - ΔV x (VRP0 + 87R + VRHP) / SUMRP	PKP4[2:0] = “111”	
KVP41	VLCD63 - ΔV x (VRP0 + 87R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	VLCD63 - ΔV x (VRP0 + 91R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “001”	
KVP43	VLCD63 - ΔV x (VRP0 + 95R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “010”	
KVP44	VLCD63 - ΔV x (VRP0 + 99R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “011”	
KVP45	VLCD63 - ΔV x (VRP0 + 103R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “100”	
KVP46	VLCD63 - ΔV x (VRP0 + 107R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “101”	
KVP47	VLCD63-ΔV x (VRP0 + 111R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “110”	
KVP48	VLCD63 - ΔV x (VRP0 + 115R + VRHP + VRLP) / SUMRP	PKP5[2:0] = “111”	
KVP49	VLCD63 - ΔV x (VRP0 + 120R + VRHP + VRLP) / SUMRP	--	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
ΔV: Voltage difference between VLCD63 and of GND.

Reference voltage of negative polarity:

Reference	Formula	Micr0-adjusting rgister	Reference voltage
KVN0	VLCD63 - ΔV x VRN0 / SUMRN	--	VINN0
KVN1	VLCD63 - ΔV x (VRN0 + 5R) / SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	VLCD63 - ΔV x (VRN0 + 9R) / SUMRN	PKN0[2:0] = “001”	
KVN3	VLCD63 - ΔV x (VRN0 + 13R) / SUMRN	PKN0[2:0] = “010”	
KVN4	VLCD63 - ΔV x (VRN0 + 17R) / SUMRN	PKN0[2:0] = “011”	
KVN5	VLCD63 - ΔV x (VRN0 + 21R) / SUMRN	PKN0[2:0] = “100”	
KVN6	VLCD63 - ΔV x (VRN0 + 25R) / SUMRN	PKN0[2:0] = “101”	
KVN7	VLCD63 - ΔV x (VRN0 + 29R) / SUMRN	PKN0[2:0] = “110”	
KVN8	VLCD63 - ΔV x (VRN0 + 33R) / SUMRN	PKN0[2:0] = “111”	
KVN9	VLCD63 - ΔV x (VRN0 + 33R + VRHN) / SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	VLCD63 - ΔV x (VRN0 + 34R + VRHN) / SUMRN	PKN1[2:0] = “001”	
KVN11	VLCD63 - ΔV x (VRN0 + 35R + VRHN) / SUMRN	PKN1[2:0] = “010”	
KVN12	VLCD63 - ΔV x (VRN0 + 36R + VRHN) / SUMRN	PKN1[2:0] = “011”	
KVN13	VLCD63 - ΔV x (VRN0 + 37R + VRHN) / SUMRN	PKN1[2:0] = “100”	
KVN14	VLCD63 - ΔV x (VRN0 + 38R + VRHN) / SUMRN	PKN1[2:0] = “101”	
KVN15	VLCD63 - ΔV x (VRN0 + 39R + VRHN) / SUMRN	PKN1[2:0] = “110”	
KVN16	VLCD63 - ΔV x (VRN0 + 40R + VRHN) / SUMRN	PKN1[2:0] = “111”	
KVN17	VLCD63 - ΔV x (VRN0 + 45R + VRHN) / SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	VLCD63 - ΔV x (VRN0 + 46R + VRHN) / SUMRN	PKN2[2:0] = “001”	
KVN19	VLCD63 - ΔV x (VRN0 + 47R + VRHN) / SUMRN	PKN2[2:0] = “010”	
KVN20	VLCD63 - ΔV x (VRN0 + 48R + VRHN) / SUMRN	PKN2[2:0] = “011”	
KVN21	VLCD63 - ΔV x (VRN0 + 49R + VRHN) / SUMRN	PKN2[2:0] = “100”	
KVN22	VLCD63 - ΔV x (VRN0 + 50R + VRHN) / SUMRN	PKN2[2:0] = “101”	
KVN23	VLCD63 - ΔV x (VRN0 + 51R + VRHN) / SUMRN	PKN2[2:0] = “110”	
KVN24	VLCD63 - ΔV x (VRN0 + 52R + VRHN) / SUMRN	PKN2[2:0] = “111”	
KVN25	VLCD63 - ΔV x (VRN0 + 68R + VRHN) / SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	VLCD63 - ΔV x (VRN0 + 69R + VRHN) / SUMRN	PKN3[2:0] = “001”	
KVN27	VLCD63 - ΔV x (VRN0 + 70R + VRHN) / SUMRN	PKN3[2:0] = “010”	
KVN28	VLCD63 - ΔV x (VRN0 + 71R + VRHN) / SUMRN	PKN3[2:0] = “011”	
KVN29	VLCD63 - ΔV x (VRN0 + 72R + VRHN) / SUMRN	PKN3[2:0] = “100”	
KVN30	VLCD63 - ΔV x (VRN0 + 73R + VRHN) / SUMRN	PKN3[2:0] = “101”	
KVN31	VLCD63 - ΔV x (VRN0 + 74R + VRHN) / SUMRN	PKN3[2:0] = “110”	
KVN32	VLCD63 - ΔV x (VRN0 + 75R + VRHN) / SUMRN	PKN3[2:0] = “111”	
KVN33	VLCD63 - ΔV x (VRN0 + 80R + VRHN) / SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	VLCD63 - ΔV x (VRN0 + 81R + VRHN) / SUMRN	PKN4[2:0] = “001”	
KVN35	VLCD63 - ΔV x (VRN0 + 82R + VRHN) / SUMRN	PKN4[2:0] = “010”	
KVN36	VLCD63 - ΔV x (VRN0 + 83R + VRHN) / SUMRN	PKN4[2:0] = “011”	
KVN37	VLCD63 - ΔV x (VRN0 + 84R + VRHN) / SUMRN	PKN4[2:0] = “100”	
KVN38	VLCD63 - ΔV x (VRN0 + 85R + VRHN) / SUMRN	PKN4[2:0] = “101”	
KVN39	VLCD63 - ΔV x (VRN0 + 86R + VRHN) / SUMRN	PKN4[2:0] = “110”	
KVN40	VLCD63 - ΔV x (VRN0 + 87R + VRHN) / SUMRN	PKN4[2:0] = “111”	
KVN41	VLCD63 - ΔV x (VRN0 + 87R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	VLCD63 - ΔV x (VRN0 + 91R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “001”	
KVN43	VLCD63 - ΔV x (VRN0 + 95R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “010”	
KVN44	VLCD63 - ΔV x (VRN0 + 99R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “011”	
KVN45	VLCD63 - ΔV x (VRN0 + 103R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “100”	
KVN46	VLCD63 - ΔV x (VRN0 + 107R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “101”	
KVN47	VLCD63-ΔV x (VRN0 + 111R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “110”	
KVN48	VLCD63 - ΔV x (VRN0 + 115R + VRHN + VRLN) / SUMRN	PKN5[2:0] = “111”	
KVN49	VLCD63 - ΔV x (VRN0 + 120R + VRHN + VRLN) / SUMRN	--	VINN7

SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1
ΔV: Voltage difference between VLCD63 and of GND.

12 MAXIMUM RATINGS

Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
VDD	Supply Voltage	-0.3 to +2.7	V
VDDIO		-0.3 to +4.0	V
VDDEXT		-0.3 to +4.0	V
VCI	Input Voltage	VSS - 0.3 to 5.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-20 to +70	°C
T_{stg}	Storage Temperature	-65 to +150	°C
Ron	Input Resistance	TBD	Ω

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that VCI and Vout be constrained to the range VSS < VDDIO ≤ VCI < V_{OUT}. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either VSS or VDDIO). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

13 DC CHARACTERISTICS

DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.5 to 3.6V, T_A = -20 to 70°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.65	-	2.5	V
VDDIO	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.16	-	3.6	V
VDDEXT	Auxiliary power supply pin for VDD	Recommend Operating Voltage Possible Operating Voltage	1.65	-	3.6	V
VCI	Booster Reference Supply Voltage Range (3)	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
VGH	Gate driver High Output Voltage		6.8	-	15.0	V
VgoffL	Gate driver Low Output Voltage		-12.6	-	-3.56	V
VcomH	Vcom High Output Voltage			TBD		
VcomL	Vcom Low Output Voltage		-VCI1+0.5	TBD		V
VLCD63	Max. Source Voltage		-	-	5.5	V
ΔVLCD63	Source voltage variation		-2		2	%
V_{OH1}	Logic High Output Voltage	Iout=-100μA	0.9* VDDIO	-	VDDIO	V
V_{OL1}	Logic Low Output Voltage	Iout=100μA	0	-	0.1*VDDIO	V
V_{IH1}	Logic High Input voltage		0.8*VDDIO	-	VDDIO	V
V_{IL1}	Logic Low Input voltage		0	-	0.2*VDDIO	V
I_{OH}	Logic High Output Current Source	Vout = V_{DD}-0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	Vout = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	μA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
f_{DOTCLK}	DOTCLK frequency	Display is ON	1		12	MHz
R_{SON}	Source drivers output resistance		-	1	TBD	kΩ
R_{GON}	Gate drivers output resistance		-	500	TBD	Ω
R_{CON}	Vcom output resistance		-	200	TBD	Ω

14 AC CHARACTERISTICS

Table 3 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DDIO} = 1.65V to 2.5V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	TBD	-	ns
t_{AS}	Address Setup Time	-	TBD	-	ns
t_{AH}	Address Hold Time	-	TBD	-	ns
t_{DSW}	Data Setup Time	-	TBD	-	ns
t_{DHW}	Data Hold Time	-	TBD	-	ns
t_{ACC}	Data Access Time	-	TBD	-	ns
t_{OH}	Output Hold time	-	TBD	-	ns

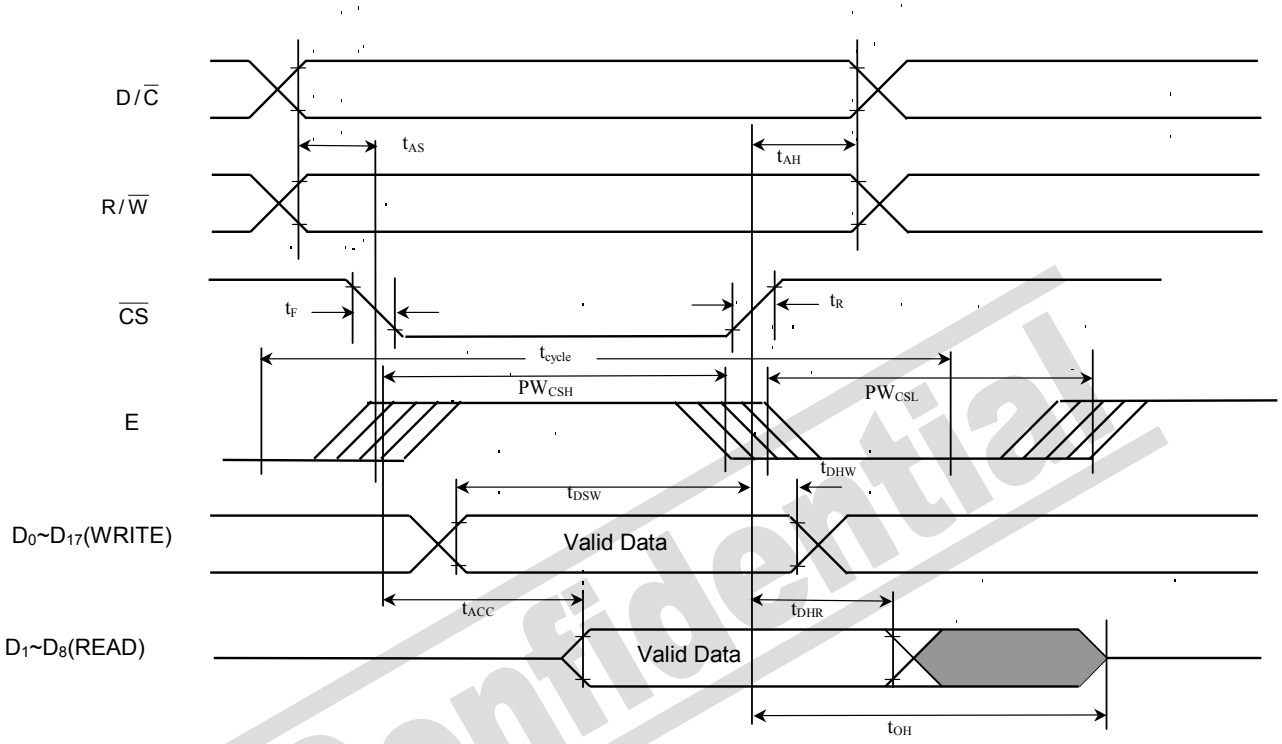
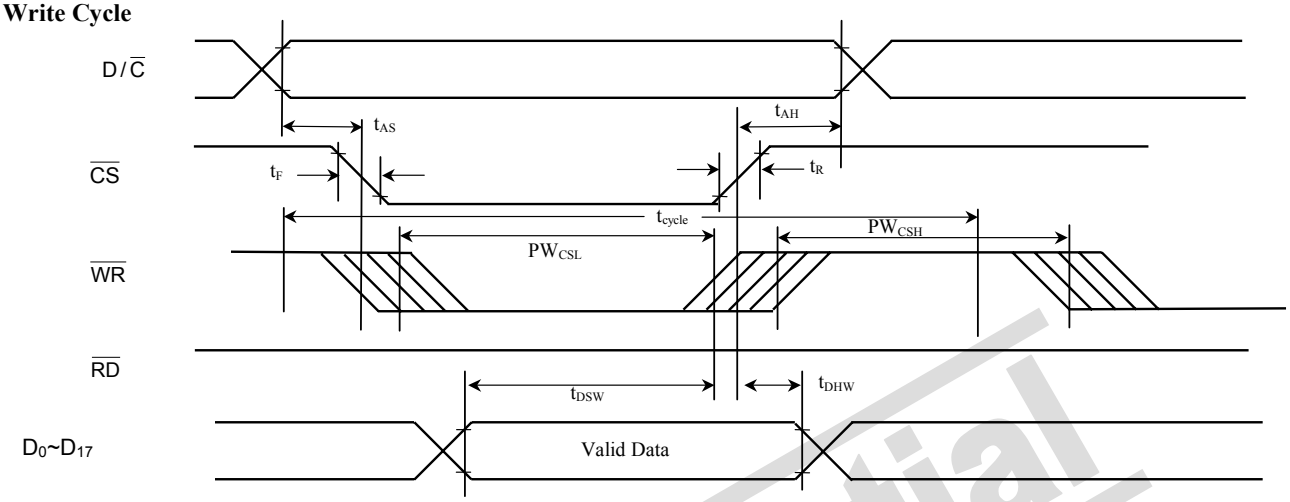


Figure 1 –Parallel 6800-series Interface Timing Characteristics

Table 4 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DDIO} = 1.65V to 2.5V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	-	TBD	-	ns
t_{AS}	Address Setup Time	-	TBD	-	ns
t_{AH}	Address Hold Time	-	TBD	-	ns
t_{DSW}	Data Setup Time	-	TBD	-	ns
t_{DHW}	Data Hold Time	-	TBD	-	ns
t_{ACC}	Data Access Time	-	TBD	-	ns
t_{OH}	Output Hold time	-	TBD	-	ns

Write Cycle



Read Cycle

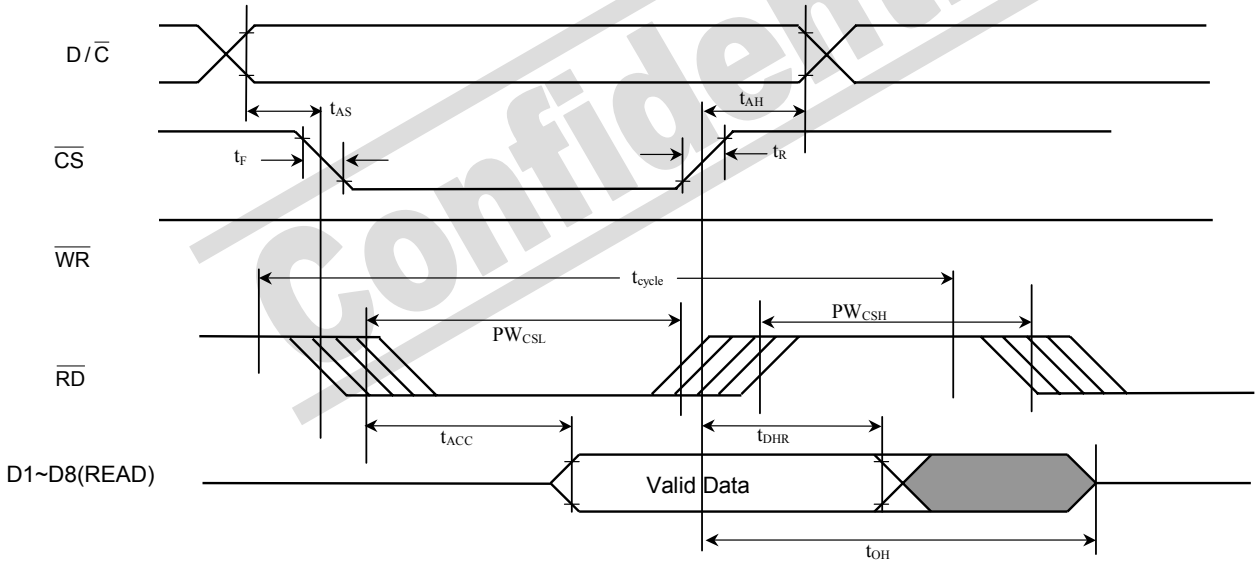


Figure 2 –Parallel 8080-series Interface Timing Characteristics

Table 5 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DDIO} = 1.65V to 2.5V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	-	TBD	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	TBD	13	MHz
t_{AS}	Register select Setup Time	-	TBD	-	ns
t_{AH}	Register select Hold Time	-	TBD	-	ns
t_{CSS}	Chip Select Setup Time	-	TBD	-	ns
t_{CSH}	Chip Select Hold Time	-	TBD	-	ns
t_{DSW}	Write Data Setup Time	-	TBD	-	ns
t_{OHW}	Write Data Hold Time	-	TBD	-	ns
t_{CLKL}	Clock Low Time	-	TBD	-	ns
t_{CLKH}	Clock High Time	-	TBD	-	ns

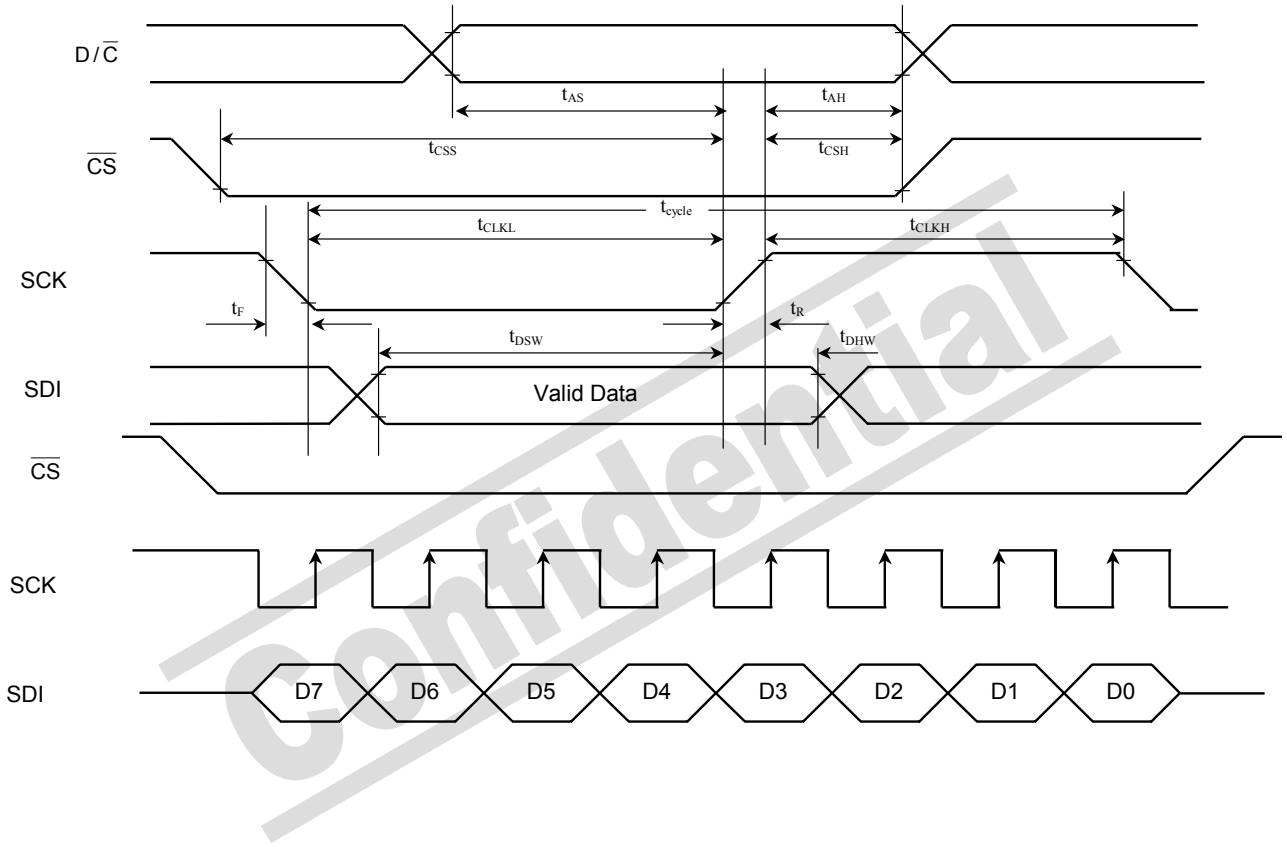


Figure 3 – 4 wire Serial Timing Characteristics

15 GDDRAM Address

	RL=1	S0	S1	S2	S3	S4	S5	S6	S7	S8	…	S390	S391	S392	S393	S394	S395	
	RL=0	S395	S394	S393	S392	S391	S390	S389	S388	S387	…	S5	S4	S3	S2	S1	S0	
	BGR=0	R	G	B	R	G	B	R	G	B	…	R	G	B	R	G	B	Vertical
	BGR=1	B	G	R	B	G	R	B	G	R	…	B	G	R	B	G	R	address
TB=1	TB=0																	
G0	G175	0000H			0001H			0002H			…	0082H			0083H			0
G1	G174	0100H			0101H			0102H			…	0182H			0183H			1
G2	G173	0200H			0201H			0202H			…	0282H			0283H			2
G3	G172	0300H			0301H			0302H			…	0382H			0383H			3
G4	G171	0400H			0401H			0402H			…	0482H			0483H			4
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.	.	.			.			.			.	.			.			.
.	.	.			.			.			.	.			.			.
G172	G3	AC00H			AC01H			AC02H			…	AC82H			AC83H			172
G173	G2	AD00H			AD01H			AD02H			…	AD82H			AD83H			173
G174	G1	AE00H			AE01H			AE02H			…	AE82H			AE83H			174
G175	G0	AF00H			AF01H			AF02H			…	AF82H			AF83H			175
Horizontal address		0			1			2			…	130			131			

Remark : The address is in yyxxH format, where yy is the vertical address and xx is the horizontal address

16 Interface Mapping

1) Mapping for Writing an Instruction

		Hardware pins																	
Interface	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
16 bits		IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8		IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
9 bits	1st										IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	x
	2nd										IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	x
8 bits	1st										IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	
	2nd										IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	

Remark : x Don't care bits

Not connected pins

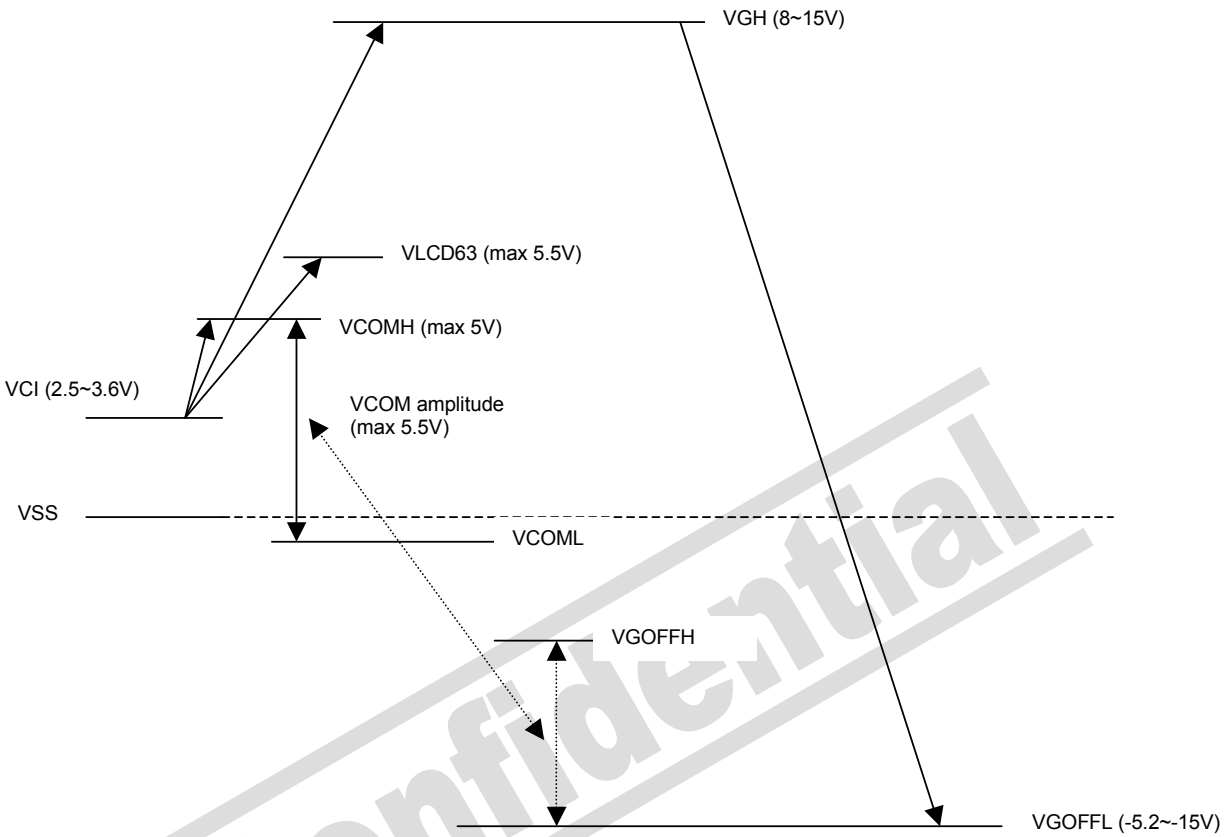
2) Mapping for Writing Pixel Data(s)

			Hardware pins																	
Interface	**Color mode**	**Cycle**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
18 bits	262k		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits	**262k**	1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		R5	R4	R3	R2	R1	R0	x	x	
		3rd	G5	G4	G3	G2	G1	G0	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	x	x	x	x	x	x	x	x		B5	B4	B3	B2	B1	B0	x	x	
		1st	R5	R4	R3	R2	R1	R0	x	x		G5	G4	G3	G2	G1	G0	x	x	
		2nd	B5	B4	B3	B2	B1	B0	x	x		x	x	x	x	x	x	x	x	
	65k		R4	R3	R2	R1	R0	G5	G4	G3		G2	G1	G0	B4	B3	B2	B1	B0	
9 bits	262k	1st										R5	R4	R3	R2	R1	R0	G5	G4	G3
		2nd										G2	G1	G0	B5	B4	B3	B2	B1	B0
8 bits	**262k**	1st										R5	R4	R3	R2	R1	R0	x	x	
		2nd										G5	G4	G3	G2	G1	G0	x	x	
		3rd										B5	B4	B3	B2	B1	B0	x	x	
	65k	1st										R4	R3	R2	R1	R0	G5	G4	G3	
		2nd										G2	G1	G0	B4	B3	B2	B1	B0	

Remark : x Don't care bits

Not connected pins

17 SSD1286 OUTPUT VOLTAGE RELATIONSHIP



18 APPLICATION CIRCUIT

Figure 3. Booster Capacitors

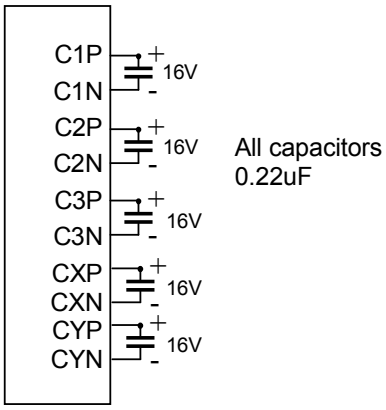


Figure 4. Filtering and Charge Sharing Capacitors

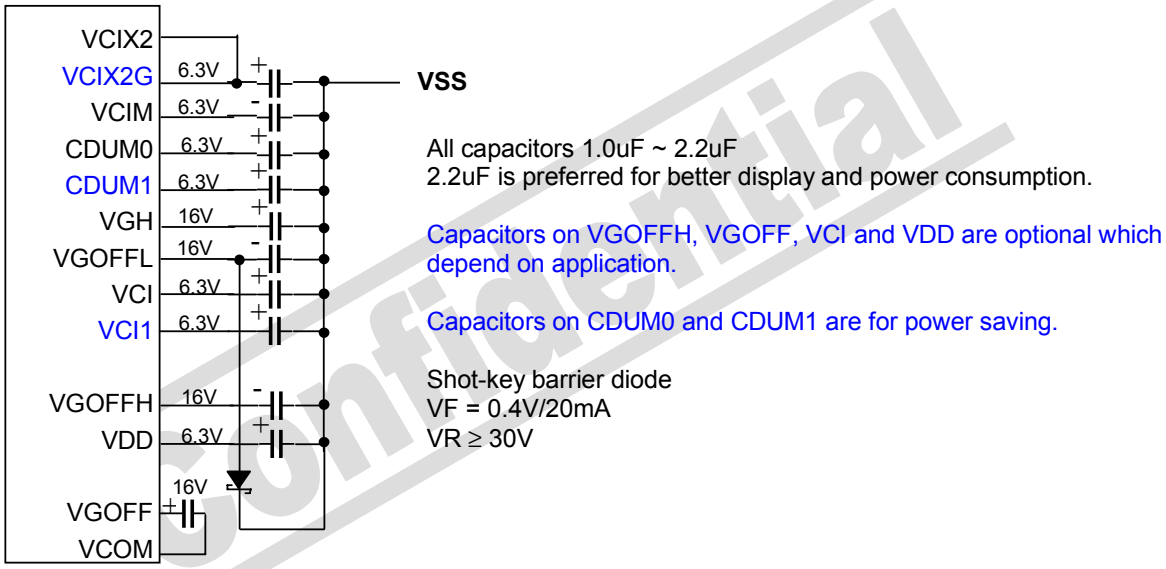
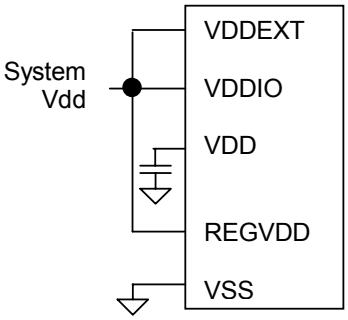
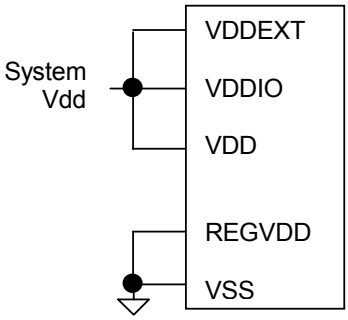


Figure 5. Power Supply Pins Connections

3.6V ≥ System Vdd > 2.5V



2.5V ≥ System Vdd > 1.65V



1.65V ≥ System Vdd > 1.16V

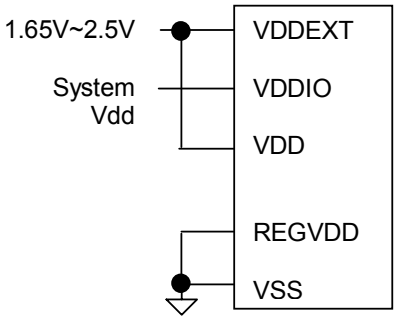


Figure 4. Panel Connection Example (with external resistor for panel trimming)