



ATA Device IP core

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Product Specification



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Features

- Support PIO modes 0, 1, 2, 3 and 4
- Support Multiword DMA modes 0, 1 and 2
- Support UDMA modes 0, 1, 2, 3, 4, 5 and 6
- Support Master/Master with Slave/Slave mode
- Support CHS, 28-bit LBA, 48-bit LBA addressing
- CRC error checking
- High performance data transfer by FIFO interface
- Compliant with ATA/ATAPI-7 Specifications.

Applications

- Solid state disk device
- Video/Image stream processing
- Embedded system requires high speed data transfer

ATA Device IP Core Facts

Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	NGC Netlist
Constraints Files	User constraint file
Verification	VHDL Test Bench
Instantiation Templates	VHDL
Reference Designs & Application Notes	None
Additional Items	None
Simulation Tool Used	
ModelSim version 6.1e	
Support	
Support Provided by Design Gateway Co.,Ltd	

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	GCLK	BRAM	MULT/DSP48/E	DCM / CMT	MGT	Design Tools
Spartan®-3E	XC3S1200E-4FG400	178	719	236	2	-	-	-	N/A	ISE® 10.1.03i
Virtex®-4	XC4VLX25-10FF668	285	720	236	2	-	-	-	N/A	ISE® 10.1.03i
Virtex®-5	XC5VLX50T-1FF1136	333	918	236	2	-	-	-	N/A	ISE® 10.1.03i

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assuming all core I/Os and clocks are routed off-chip

December 01, 2008

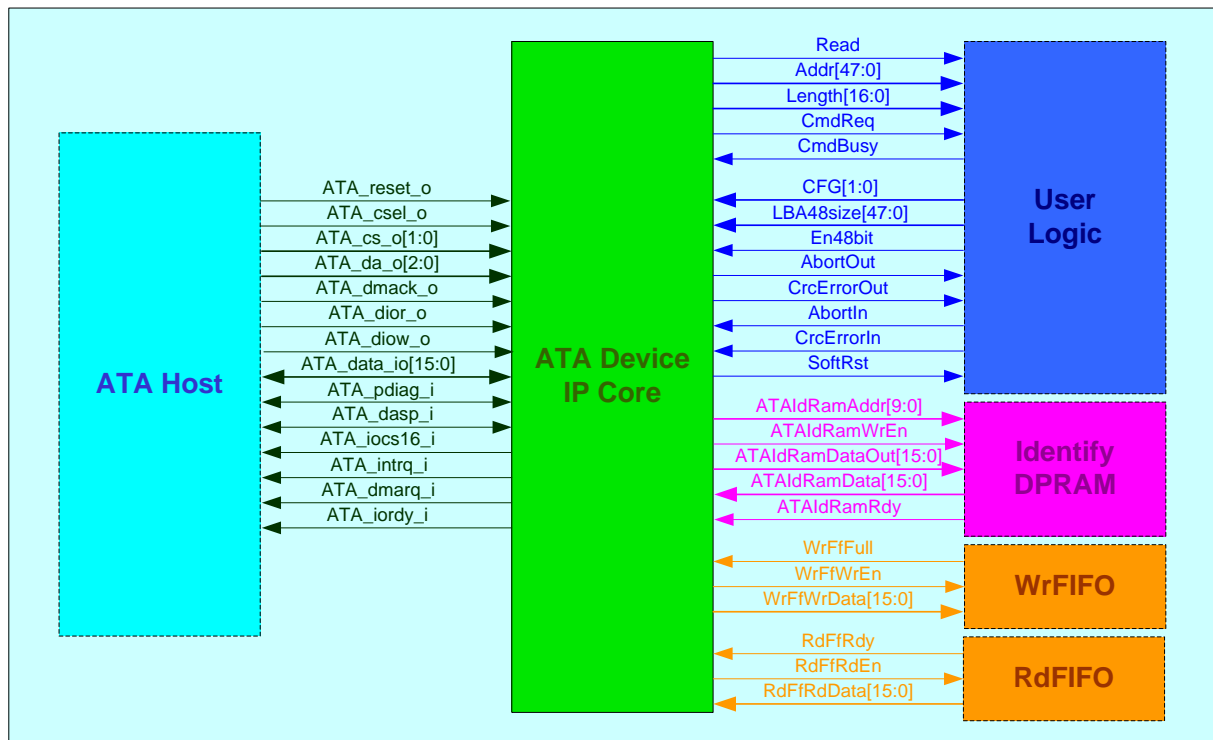


Figure 1: ATA Device IP core Block Diagram

General Description

ATA device IP core is designed to interface between ATA host system and user storage system. ATA command from host system is handled and translated to simple control signals by ATA device IP core. Data burst transfer is achieved by using FIFO interface, while identify device data is transferred through Dual-Port RAM interface to provide user system setting disk information such as disk size, name, serial number. Abort flag and CRC error flag, directly mapped from register inside ATA device IP core, can be monitored and controlled by user system.

Functional Description

ATA device IP user interface signals are designed to transfer two types of data, i.e. identify device data from DPRAM and standard data from two FIFOs. More details about these data are described as follows.

Identify Device

When ATA host system sends identify device command to ATA device IP core, 512-byte data from Identify DPRAM will be read and returned to host system. So user system needs to prepare all identify device data storing to DPRAM and set ATAIdRamRdy to '1' to notify IP core that data is ready. Host system will not get any identify device data unless ATAIdRamRdy is set from user system. Identify data consists of disk information such as number of logical cylinders, serial number, firmware revision, model number, current capacitor in sector, total number of user addressable sectors, supported 48-bit address, and maximum user LBA for 48-bit address.

Standard Data

When ATA host system sends write/read command to ATA device IP core, IP core will send start address, transfer size, transfer direction from host system to user logic. Data transfer will start after CmdBusy is set by user logic and FIFO flag is in ready state.

For write transfer, data from host will be stored to WrFIFO in sector unit. WrFfFull will be monitored by IP core after each sector is written to FIFO. ATA device IP core will pause data from host system if WrFfFull is set to '1'.

For read transfer, data from RdFIFO will be transferred to host in sector unit. Similar to write transfer, RdFfRdy will be monitored and no data transfer to host unless RdFfRdy is set to '1'.

After all data transfer from/to FIFO completely, ATA device IP core will be in Busy state until CmdBusy from user logic is released to '0'. Abort signal from IP core will be set if host system sends some error data such as wrong CRC, not supported command, and access out of range of system address.

Core Modifications

ATA Device IP core can customized to meet with specific speed/delay requirement. Please contact Design Gateway Co.,Ltd for any required modifications.

Core I/O Signals

The core signals I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
ATA Interface		
ATA_reset_o	Input	ATA reset. Reset signal from ATA bus
ATA_csel_o	Input	ATA cable select
ATA_cs_o[1:0]	Input	ATA chip select
ATA_da_o[2:0]	Input	ATA address
ATA_dmack_o	Input	ATA DMA acknowledge
ATA_dior_o	Input	ATA I/O read
ATA_diow_o	Input	ATA I/O write
ATA_data_io[15:0]	Inout	ATA data bus
ATA_pdiag_i	Inout	ATA passed diagnostics
ATA_dasp_i	Inout	ATA device active or slave (Device1) present
ATA_iocs16_i	Output	ATA I/O control signal. Indicates that data width between host and device is 16 bits
ATA_intrq_i	Output	ATA interrupt request
ATA_dmarq_i	Output	ATA DMA request
ATA_iordy_i	Output	ATA I/O ready
User Control Section		
RstB	Input	System Reset signal (Active Low)
Clk	Input	System clock (133 MHz)
Read	Output	Transfer direction ('0': Write data to WrFf, '1' Read data from RdFf)

ATA Device IP core

Addr[47:0]	Output	Start transfer address in sector unit (512 bytes)
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Signal	Signal Direction	Description
Length[16:0]	Output	Transfer Length in sector unit (512 bytes)
CmdReq	Output	Data transfer request
CmdBusy	Input	Data transfer busy (acknowledge)
CFG[1:0]	Input	ATA configuration mode ("00": Master, "01": Master with slave present, "11": Slave, "10": Preserved)
LBA48size[47:0]	Input	Disk size in sector unit (512 bytes) for detect out of range area access
En48bit	Input	Enable LBA mode ('0': CHS/28 bit LBA mode, '1': 48 bit LBA mode)
AbortOut	Output	Abort flag in status register inside IP core ('0': Normal, '1': Abort)
CrcErrorOut	Output	CRC error in ATA bus ('0': No error, '1': Error)
AbortIn	Input	Force Abort flag to be '1' ('0': Disable, '1': Force Abort to '1')
CrcErrorIn	Input	Force CrcError flag to be '1' ('0': Disable, '1': Force CrcError to '1')
SoftRst	Output	Software reset
Identify Device Section		
ATAIdRamAddr[9:0]	Output	Identify device RAM address
ATAIdRamWrEn	Output	Identify device data write enable ('0': No action, '1': Write data to RAM)
ATAIdRamDataOut[15:0]	Output	Identify device data output
ATAIdRamData[15:0]	Input	Identify device data input
ATAIdRamRdy	Input	Identify device data ready ('0': Data not ready, '1': Data ready)
Standard Data Section		
WrFfFull	Input	WrFifo full flag. Set to '1' when remain space is less than 1024 bytes
WrFfWrEn	Output	WrFifo data write enable ('0': No action, '1': Write data to WrFifo)
WrFfWrData[15:0]	Output	WrFifo data input
RdFfRdy	Input	RdFifo data output ready. Set to '1' when data remain at least 512 bytes or when all data are stored inside RdFifo.
RdFfRdEn	Output	RdFifo data read enable ('0': No action, '1': Read data from RdFifo)
RdFfRdData[15:0]	Input	RdFifo data output

Verification Methods

The ATA Device IP core functionality was verified with function simulation model and static timing analysis. The board-level timing has been verified with real hardware measurements using several in-house developed boards. The ATA Device IP core is in use by customers using Xilinx FPGA devices.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available directly from Xilinx Alliance Program member, Design Gateway Co.,Ltd
Please contact Design Gateway Co.,Ltd for pricing and additional information about this product
using the contact information on the front page of this datasheet.

Related Information

American National Standard Institute.

For information on ATA/ATAPI-7 specification

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