COMPUWARE
肯 微 科 技 股 份 有 限 公 司

Document Name
Product Specification

Release Document

Compuware Project Name	**CPR-9211-1M1LF**	Revision	**1**
Customer Project Name		Date	**2012/03/12**
Component P/N		Page	**19**

History Record		
Date	Description	Revision
2010/01/26	新製定	0
2012/03/12	Take out 920P-SQ and mention DCGOOD timing 40-100ms	1

Approved By	**Signing By**	**Prepared By**
_____		_____

1 Scopes and Definition

This specification defines the performance characteristics of a single-phase (3-wire) 920W single output power supply with wide range input AC capability (100-240VAC/50-60Hz) under operation temperature 50 degree C. The power supply shall be designed for parallel operation. In the event of a power supply failure, the redundant power supply continues to power the system even under over voltage fault. The number of power supplies per system will be limited to a maximum of three. The power supply shall be designed for “hot swap” exchange and must contain the OR-ing isolation MOSFETs for all outputs and shall communicate to external devices through Inter-Integrated (I2C) Circuit protocol. The power supply will have an EEPROM for storing powers supply FRU information, and meet PMBusRevision 1.2 requirement.

2 Input Requirement

2.1 AC Input Requirements

The power supply must operate within all specified limits over the following input voltage range. Harmonic distortion of up to 10% THD must not cause the power supply to go out of the specified limits. 5% is our target at full load and 10% at 20% load with 230VAC input. The power supply shall operate properly at 87 VAC input voltage to guarantee proper design margins.

The Power supply must be have a universal power input with active power correction to reduce the line harmonics in accordance with the EN61000-3-2 standard, see section 9 for detailed regulatory standards.

The power supply must be capable of operating with the following Conditions

	Minimum	Nominal	Maximum	Unit
Input Voltage Range(Vac)	85	100/240	264	Vac
Input Frequency(Hz)	47	60/50	63	Hertz
Input Current(A)	13.5	11/4.5	4	Amperes

The unit must not go into hiccup mode when in the boundary of Turn on voltage threshold, an ACUV circuit is recommended.

2.2 Power Factor

The power supply must have a minimum 0.96 and 0.98 at 115Vac measured with 40% and 80% load respectively; and minimum 0.9, 0.92 and 0.96 at 230Vac measured with 20%, 50%, and 100% load respectively.

2.3 Inrush Current

When input power is applied to the power supply any initial current surge or spike of 10ms or less will not exceed 25A peak. Any additional inrush current surges or spikes in the form of AC cycles or multiple AC cycles greater than 10ms, and less than 150ms, must not exceed 15A peak. After 150ms the AC input current must meet the input AC current requirements 2.1

For any conditions during turn-on the inrush current will not open the primary input fuse or damage any other

components.

2.4 Efficiency

The Power supply must have a minimum of 90% Efficiency measured at 20% output loading with nominal input AC voltage condition (110~240Vac). It shall have minimum 94% peak efficiency for 230Vac input without fan power. Also efficiency should be meet climate saver targets Platinum level as below (AC input 230Vac only).

Loading(without fan power)	Efficiency	PF
10%		
20%	90%	
50%	94%	0.9
100%	91%	

2.5 Input fuse

The Input fuse must be slow blow or normal blow high breaking type.

2.6 Input Receptacle

The AC input receptacle must be approved by Product Safety Regulatory Agencies and must be rated properly for current, voltage and temperature. The AC input connector shall be an IEC 320 C-14 power inlet.

2.7 Input Under Voltage

The power supply shall contain protection circuitry such that application of an input voltage below the minimum specified in section 2.1 shall not cause damage to the power supply. Input voltage range for AC minimum startup voltage, 84-89VAC, and maximum turn off voltage range 79 to 83VAC.

2.8 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions. Sag conditions (also referred to as “brownout” conditions) will be defined as the AC line voltage dropping below nominal voltage. Surge will be defined as the AC line voltage rising above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 1: AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
0 to 1 AC cycle	100%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance with system load.
> 1 AC cycle	>10%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self-recoverable

Table 2: AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria

Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

2.9 AC Line Fast Transient Specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-45:1995 and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum output load conditions.

3 Output Requirements

3.1 Output regulation Requirements

All outputs must maintain their regulation with the below limits when measured at the output connector point or across the remote sense (if applicable) in any load condition defined in **section 3.2**

Output	Minimum	Nominal	Maximum	Unit
+12V	11.40	12.0	12.60	Vdc
+5Vsb	4.80	5.0	5.25	Vdc

+12V output voltages must lower than 0.35V and better be less than 0,1V when stay with 5Vsb.

3.2 Output Current Requirements

All outputs must maintain their regulation as per **section 3.1** when loaded to the following loading combination:

Output	Minimum	Maximum	Unit	Input VAC
+12V	0.5	75	Adc	90 to 140
+5Vsb	0	4.0	Adc	90 to 140
+12V	0.5	75	Adc	180 to 264
+5Vsb	0	4.0	Adc	180 to 264

The total output power can not exceed 920W continuously for 90 to 264VAC input. During load changes from minimum to maximum or maximum to minimum the unit must not shut down.

3.3 Output Ripple and Noise

The following output ripple/noise requirements will be met throughout the load ranges specified in **section 3.2** and under all input voltage conditions specified in **section 2.1**.
Ripple and noise are defined as periodic or random signals over the frequency band of 10Hz to 20MHz. Measurements will be made with an oscilloscope set to 20MHz bandwidth limit. Measurement is done by using 10uF Tantalum in parallel with a 0.1uf ceramic capacitor, measured directly at the output connector side (Note: care must be taken when doing measurements such as using the smallest grounding wire.).

Output	Maximum	Unit
+12V	120	mV
+5Vsb	50	mV

3.4 Output Dynamic Loading

The output voltages shall remain within the limits specified in **section 3.1** for the step loading and within the limits specified in **section 3.5** for the capacitive loading. The load transient repetition rate shall be tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load shown in **section 3.2**

3.4 Transient Load Requirements

Output	Δ Step Load Size	Load Slew Rate	Capacitive Load
12V	65% of max load	0.5 A/μs	2200 μF
+5 VSB	25% of max load	0.5 A/μs	1 μF

3.5 Capacitive Loading

The power supply shall be stable and meet all requirements, except dynamic loading requirements, with the following capacitive loading ranges.

3.5 Capacitive Loading Conditions

Output	MIN	MAX	Units
+12 V	10	11,000	μF
+5 VSB	1	350	μF

4 Redundancy Requirements

4.1 Current Sharing Operation

The power supply shall be designed for active current sharing.
Two or more than two power supplies will be paralleled in a system. Each power supply must be able to share load to within +/-10 % share error measured 25, 50, 100% of single power supply full load current.
5Vsb requires an “ORing” diode or FET to provide protection against internal short circuit fault.

4.2 Output Isolation Oring MOSFET

The 12V output current must pass through an Oring MOSFET to protect the bus voltage against a power supply internal fault.

4.3 Power Supply Behavior When Faulted

1 The faulted supply shall not sink more than 100 mA current.
2 I2C bus status shall be operational and valid, refer to “**I2C Bus/VPD** Interface”.
3 The "DC Good" signal and "DC Good Fault" bit status shall be valid.
4 A power supply that fails due to a 12V or 5Vsb Over-Voltage condition will shutdown gracefully and will not cause shutdown of the other power supplies in parallel.
5 The power supply has to save 5 latest records of the abnormal shutdown on the EEPROM. The record is a byte data format, and its definition is shown below. The record should be clear before the shipping.

```
#define (reserved)          0x01
#define PRIMARY_OTP         0x02
#define SECONDARY_OTP       0x03
#define (reserved)          0x04
```

```
#define SCP_FAULT              0x05
#define OCP_FAULT_220V         0x06
#define OCP_FAULT_110V         0x07
#define OVP_FAULT              0x08
#define DC12V_OVP_FAULT        0x09
#define DC12V_UVP_FAULT        0x0A
#define AC LOSS                0x0B
#define FAN2_FAULT             0x0C
#define FAN1_FAULT             0x0D
#define OPP_FAULT              0x0E
#define OTHER_FAULT            0x0F
```

4.4 Parallel Stability

The power supply shall be unconditionally stable under all system load and AC line conditions while operating alone or in parallel mode.

4.5 Hot Swap

The power supply must be designed with “hot swap” function with or without active AC line cord. After Hot swap I2C address shall be same as host power supply backplane hardware assigned. Host existing working power supply shall not be affected by hot swapping power supply.

5 Controls and Signal

5.1 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 13 ms.

Each output voltage shall reach regulation within 50 ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400 ms (T_{vout_off}) of each other during turn off. Figure 1 and Figure 2 the turn ON and turn OFF timing requirements. In Figure 2, the timing is shown with both AC and PSON# controlling the ON/OFF of the power supply.

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	13	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		13	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms

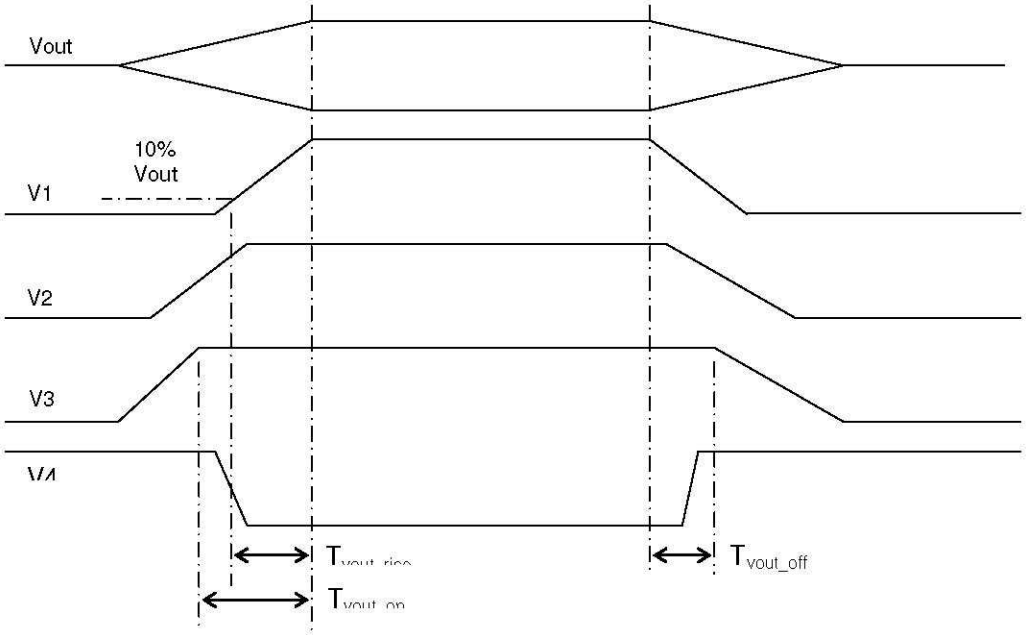


Fig. 1 Output Voltage Timings

AC Input

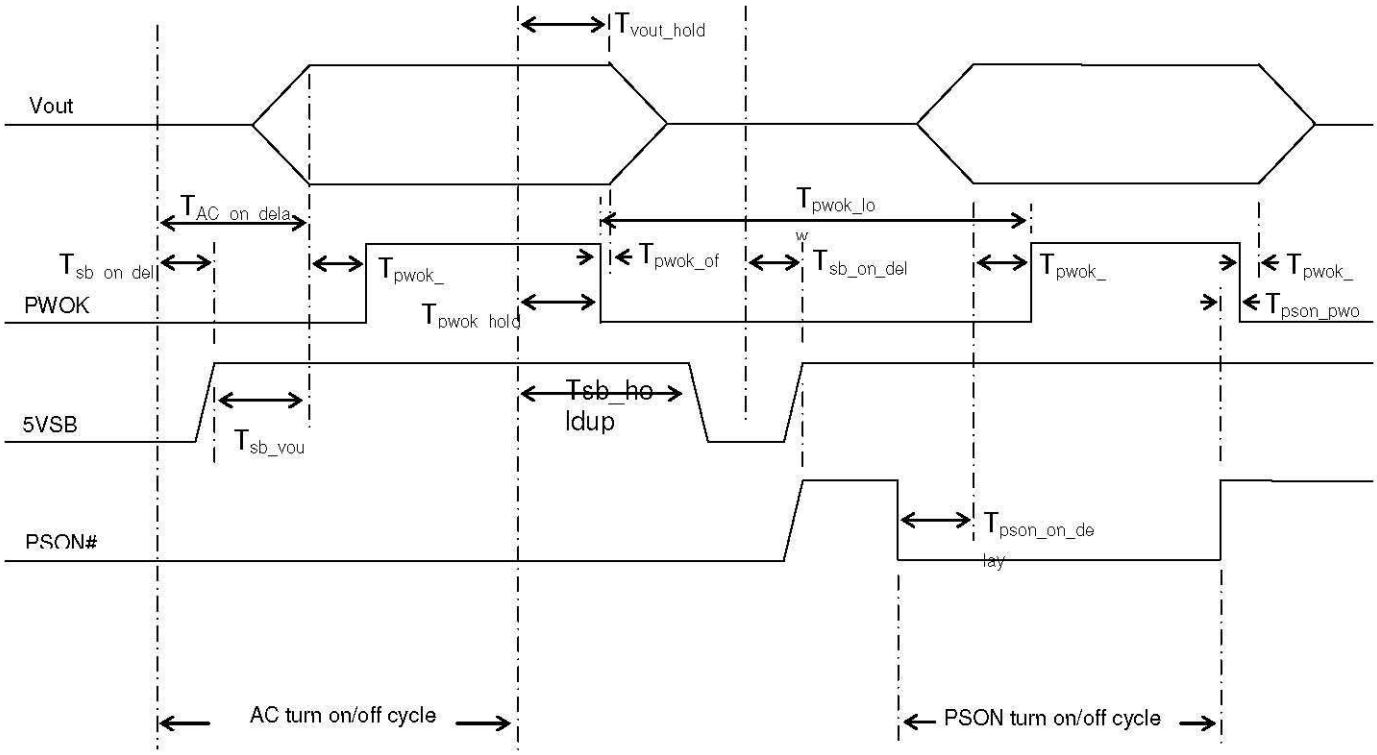


Figure 2 Turn On/Off Timing (Signal Power Supply)

Item	Description	MIN	MAX	Units
Tsb_on_delay	Delay from AC being applied to 5 VSB being within regulation.		1500	ms

T ac_on_delay	Delay from AC being applied to all output voltages being within regulation.		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC. Tested at 75% of maximum load and over 100-240VAC input	20		ms
				ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tsb_vout	Delay from 5 VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{sb_holdup}	Time 5VSB output voltage stays within regulation after loss of AC.	70		ms

5.2 PS_ON/OFF

The **ON/OFF#**" signal is an active low input used to activate the power supply 12 output voltage. If AC input is already applied, the 12V output shall be within regulation no less than 100ms after **ON/OFF#** is pulled low. When this signal is HIGH the power supply must remain off.

The PSONsignal is required to remotely turn on/off the power supply. PSONis an active low signal that turns on the +12 V power rail. When this signal is not pulled low by the system, or left open, the outputs (except the +5 VSB and Vbias) turn off. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply.

Table 3: PSONSignal Characteristic

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = Open or High	OFF	
	MIN	MAX
Logic level low (power supply ON)	0 V	1.0 V
Logic level high (power supply OFF)	2.0 V	5.25 V
Source current, Vpson = low		4 mA
Power up delay: $T_{pson\_on\_delay}$	5 ms	400 ms
DCGOOD delay: T_{pson_pwok}		50 ms

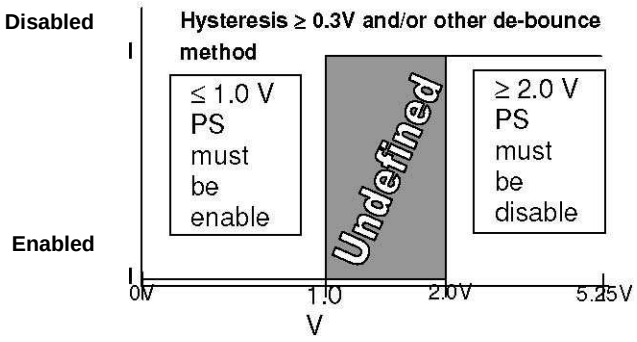


Fig.3 Logic level definition

5.3 DC GOOD

The power supply shall provide an output signal, "**DC GOOD**", which indicates that the 12V output is within the OV/UV limits.

Note: The "**DC GOOD**" signal shall be terminated at near of the output power supply connector with a 0.01 uF ceramic capacitor to filter out unwanted noise voltage.

DC GOOD (high +12V and low 0V) Delay from PSON# deactive to DC GOOD being deasserted 40-100ms. Delay from loss of AC to deassertion of DC GOOD. Tested at 75% of maximum load and over 100-240VAC input **minimum 19ms.**

Table 4: DCGOOD Signal Characteristics

Signal Type	+12V TTL Compatible output signal	
DCGOOD = High (+12V)	Power DC GOOD	
DCGOOD = Low (0V)	Power DC not GOOD	
	MIN	MAX
Open collector DC Good → signal pulled high that delayed from +12V regulation	40ms	100ms

5.4 AC Warning

Noted on PMBus standard.

5.5 LED Indicator

A green/amber double color Light Emitting Diode (LED) shall be mounted as indicated in mechanical drawing and shall indicate the status of the DC GOOD signal with green color. The LED shall continue to glow under normal operation of the power supply. If this LED is blinking or not lit or in amber color, the power supply is not operating properly.

6 I²C and PMBus™ 1.2 standard.

6.1 I²C to meet Super Micro standard.

This power support supports both Super Micro I2C function and PMbus. With different addressing, the user should able to use either Super Micro I2C FRU or PMbus commands.

6.1.1 Super Micro I2C

Slave address will be 0x70 (default).

The power supply can be read and written to as if it's an 2k bit (256 byte) I2C EEPROM. The power supply must support: Byte write and Random read. Read and write must work at speeds up to 100 kHz. This bus shall operate at 3.3V but be tolerant of 5V signaling.

All the data stored in the power supply follows FRU spec, IPMI, Platform Management FRU information Storage Definition v1.0.

FRU spec attached below:

17. FRU Information Layout 15

18. Record Field Definitions 16

18.1 Power Supply Information (Record Type 0x00) 16
18.1.1 Overall Capacity in Watts 16
18.1.2 Peak VA 17
18.1.3 Inrush 17
18.1.4 Inrush interval 17
18.1.5 Low end Input voltage range 1 17
18.1.6 High end Input voltage range 1 17
18.1.7 Low end Input voltage range 2 17
18.1.8 High end Input voltage range 2 17
18.1.9 Low end input frequency range 17
18.1.10 High end input frequency range 17
18.1.11 A/C dropout tolerance 17
18.1.12 Binary flags 17
18.1.12.1 Tachometer pulses per rotation/Predictive fail polarity 17
18.1.12.2 Other Binary flags 18
18.1.13 Peak Wattage 18
18.1.14 Combined Wattage 18
18.1.15 Predictive fail tachometer lower threshold 18
18.2 DC Output (Record Type 0x01) 19
18.2.1 Output Information 19
18.2.2 Nominal voltage 19
18.2.3 Maximum negative voltage deviation 20
18.2.4 Maximum positive voltage deviation 20
18.2.5 Ripple and Noise pk-pk, 10Hz to 30MHz 20
18.2.6 Minimum current draw 20
18.2.7 Maximum current draw 20
18.3 DC Load (Record Type 0x02) 20
18.3.1 Output Information 20
18.3.2 Nominal voltage 20
18.3.3 Spec'd minimum voltage 20
18.3.4 Spec'd maximum voltage 21
18.3.5 Ripple and Noise pk-pk 10Hz to 30MHz 21
18.3.6 Minimum current load 21
18.3.7 Maximum current load 21
18.4 Management Access Record (Record Type 0x03) 21
18.4.1 Example 22
18.5 Base Compatibility Record 24

The “Chassis Info” and “Board Info” are not to be implemented. The “Common Header” and “Product Area” are required.

For the “Multiple Record” area, the power supply should implement the “Power Supply Information”(section 18.1), and multiple “DC Output” section as needed.

For the “Product Info” area must began from offset location 0x18 (offset 0x04 product information offset must contains value of 0x03).

The “Internal Use” section, defined by Supermicro as follows:

Offset		Result of a read
0x09	Temperature	Value to represent the current temperature of the hottest spot inside the power supply This is an unsigned integer value in Celsius.
0x0A	Fan 1 speed (main fan)	Value to represent the RPM of the power supply fan #1 This should be the fan pulse count in 262 ms. We are assuming that two fan pulses equal one rotation. The system software will convert this value, to fan RPM, using: RPM=(1/0.262) *(Fan Pulse Count * 60 /2)
0x0B	Reserved	
0x0C	Power Status	Value to represent DC GOOD status byte = hex 01 means DC GOOD

		byte = 00 means no DC output
0x0D	Temperature High Limit	Value is fixed and should be the highest acceptable temperature that the power supply can sustain based on offset 09.
0x0E	Fan 1 speed Low Limit	Value is fixed and should be the lowest fan #1 RPM acceptable
0x0F	Reserved	
0x10	Reserved	
0x11	Reserved	
0x12	Reserved	
0x13	Reserved	
0x14	AC RMS current	This byte, divided by 16, is the AC (RMS) input current.
0x15	Reserved	
0x16	Firmware version	Example: version 2.0 is encoded as 0x20 The smallest version number allowed is 2.0 Anything less than 2.0 (0x20) found at this location will be reported as version 1.0 by Supermicro health monitoring software
0x17	FRU file revision	Integer only
0xF0	AC current limit	AC current upper limit; same scale factor as 0x14
0xF1	+12V DC current limit	+12V DC current upper limit; scale factor: this byte, divided by 2, is the DC (+12V) output current.
0xF2	Power supply wattage	Power supply wattage; lower byte
0xF3		Power supply wattage; higher byte
0xF4	Input voltage	100-240Vac input voltage reading
0xF5	Input power	Input power in watt (lower byte) (0x0864=360W)
0xF6	Input power	Input power in watt (higher byte)
0xFF	Write protection Control	This byte controls whether the FRU is writeable or read only. When this byte content is 0x88, the FRU is writeable. Otherwise, only byte 0xFF can be modified. value= 0x88 is FRU writeable mode Any other value, FRU is read only except address 0xFF can be modified. Default value for this byte is read only, 0x00.

The power supply will support the “byte write” procedure defined in the I2C EEPROM spec.

Read only bytes --- writes to the following bytes should be ignored:

Offset	
0x09	Temperature
0x0A	Fan 1 speed (main fan)
0x0B	Fan 2 speed (secondary fan if available)
0x0C	Power Status
0x14	AC RMS current
0xF4	Input voltage
0xF5	Input power (lower byte)
0xF6	Input power (higher byte)

I2C auto-recovery feature:
In a normal I2C transaction, there will be 8 bytes of transmission plus an ACK (acknowledge) byte, for a total of 9 clock cycles. ACK is done by pulling down the SDA line. If there is a missing clock cycle, the chip doing the ACK will hold down the SDA line indefinitely and hanging the I2C bus. The power supply needs to prevent the above scenario from happening. If the I2C bus SDA or SCL is stuck low for more than 40 ms, the power supply should reset either its I2C communication module, or itself.

The power supply I2C microcontroller should not latch the system I2C bus by pulling SDA or SCL line low for more than 40 ms.

The power supply needs to have 2k Ohm internal pull up on the SDA or SCL lines and operate at 3.3V voltage.

6.1.2 PMBus

The PMbus firmware version of the power supply shall follow the
1. PMBus Power System Management Specification Part I – General Requirements, Transport and Electrical Interface.
2. PMBus Power System Management Specification Part II – Command Language

The device in the power supply shall be compatible with both SMBus 2.0 ‘high power’ specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V but be tolerant of 5V signaling.

One pin is the Serial Clock [SCL] (PSM Clock). The second pin is used for Serial Data [SDA] (PSM Data). Both pins are bi-directional, open drain signals, and are used to form a serial bus. The circuits inside the power supply shall derive their power from the standby output.

The device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >40ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications, but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or

other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

6.1.2.A Addressing

System addressing Address2/Address1/Address0	0/0/0	0/0/1	0/1/0	0/1/1
Power supply PMBusTM device	78h	7Ah	7Ch	7Eh

Note: Non-redundant power supplies will use the 0/0/0 address location.

6.1.2.B Command

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power.

PMBus command	Description
READ_IIN	RMS input current in amps (note; not used on power distribution boards)
READ_VIN	RMS input voltage in volts(note; not used on power distribution boards)
READ PIN	AC input power in watts (note; not used on power distribution boards)
VOUT_MODE	command to report the output voltage formatting for the READ_VOUT command.
STATUS_BYTE	command to report the On/off status of the power supply. Please refer to page 72 of PMbus spec part 2

STATUS_BYTE: Please refer to PMbus part 2 spec page 72.

STATUS_BYTE Offset 0x78		
Bit #	7	Not used, default=0
	6	Device is off due to PSON or for any reason (ex. Protection)=1, else 0
	5	Output OVP=1, else 0
	4	Output OCP=1, else 0
	3	Vin under voltage=1, else 0
	2	OTP=1; else 0
	1	Not used, default=0
	0	none of the above (Power is good and turned on)=1, else=0

6.1.2.C Sensor Sampling

The sensor registers inside the power supply for monitoring input/output power, current, and voltage shall meet the following minimum requirements. Register refresh rate is the frequency the sensor register gets updated with a new measurement value. Sensor averaging duration is the time over which the data shall averaged to obtain the value of the registers value.

Register refresh rate ≥ 10Hz
Sensor averaging duration; ≤ 100msec, ≥ 10msec

6.1.2.D Accuracy

The sensor commands shall meet the following accuracy requirements.

	> 20% of max load	20%~100% of max laod
READ_IIN	+/-4% (Recommend) +/-6% (Request)	+/-2% (Recommend) +/-4% (Request)
READ_PIN	+/-4% (Recommend) +/-10% (Request)	+/-3% (Recommend) +/-5% (Request)
READ_IOUT	+/-2% (Recommend)	+/-2% (Recommend)

	+/-4% (Request)	+/-3% (Request)
READ_POUT	+/-3% (Recommend) +/-5% (Request)	+/-3% (Recommend) +/-4% (Request)
READ_VIN	+/-2% over full range (Recommend) +/-3% over full range (Request)	
READ_VOUT	+/-2% over full range	
READ_TEMPERATURE	Desired: +/-1ºC Required: +/-3 ºC	

Note: * The recommend level should cover 90% production.

7 Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shutdown. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 10 seconds and a PSONcycle HIGH for 1 second shall be able to reset the power supply.

7.1 Over Current Protection

The power supply shall have current limit to prevent +12 V outputs from exceeding the values shown in Table 5. If the current limits are exceeded, the power supply shall shutdown and latch off in timing as long as good (about 200ms) with no damage occur to PDB self and power supply. The latch will be cleared by toggling the PSONsignal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. 5 VSB shall be protected under over current or shorted conditions so that no damage can occur to the power supply. All outputs shall be protected so that no damage occurs to the power supply under a shorted output condition.

Table 5: Over Current Protection

Voltage	Over Current Limit (Iout limit)
+12 V	110% minimum; 130% maximum
+5Vsb	110% minimum;130% maximum

7.2 240VA Protection

Not applicable

7.3 Over Voltage Protection

The power supply over voltage protection shall be locally sensed. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSONsignal or by an AC power interruption. Table 6 contains the over voltage limits. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Table 6: Over Voltage Limits

Output Voltage	MIN (V)	MAX (V)
+12 V	13.3	14.5
+5 VSB	5.7	6.5

7.4 Over Thermal Protection

The power supply over thermal protection shall be locally sensed. The power supply shall shutdown and latch off after an over required temperature condition occurs. This latch shall be cleared by toggling the PSONsignal or by an AC power interruption. The over thermal limits that power supply which components contain required maximum temperature. The temperature shall never exceed the maximum levels when

measured at the individual component.

7.5 Short Circuit Protection

All outputs shall be protected and into latch off mode so that no damage occurs to the power supply under a shorted output condition. This latch shall be cleared by toggling the PSONsignal or by an AC power interruption. 5Vsb should be protected and into hiccup mode. No damage occurs to the power supply under a shorted output condition, and should be output normally after shorted output released.

8 Environmental Requirements

8.1 Temperature

8.1.1 Normal Operating Ambient(at sea level):

0 degrees Celsius minimum (operating and in standby) 50 degrees Celsius maximum (operating – power supply on)

maximum rate of change is 30 degrees Celsius/hour

8.1.2 Abnormal Operating Ambient(at sea level):

N/A degrees Celsius
N/A survival time

8.2 Humidity

Operating : 20% to 95% RH
Storage : 5% to 95% RH

8.3 Altitude

Operating: to 10,000 feet (3,023 meters)

Non-operating: to 35,000 feet (10,580 meters)

8.4 SHOCK AND VIBRATION

8.4.1 Mechanical Shock

The device will withstand the following imposed conditions without electrical or mechanical failure:
Non-operating Square Wave Shock: 40G, Square wave at 200in/sec (508cm/sec); on all six sides
Non-operating Half Sine Shock: Half Sine pulse for 70in/sec (178cm/sec) for 2ms; on all sides except top
Operating Half Sine Shock: Half Sine pulse for 40in/sec (102cm/sec) for 2ms; on all sides except top

8.4.2 Vibration

Operating: Sinusoidal vibration, 0.5G (0-peak) acceleration. 3-500Hz, sweep at 1/2 octave/min from low to high frequency, and then from high to low. Thirty minute dwell at all resonant points, where resonance is defined as those exciting frequencies at which the device under test experiences excursions two times larger than non-resonant excursions.

Plane of vibration to be along three mutually perpendicular axis.

Non-operating: Sinusoidal vibration, 1.0G (0-peak) acceleration. 3-500Hz, sweep at 1/2 octave/min from low to high frequency, and then from high to low. Thirty minute dwell at all resonant points, where resonance is defined as those exciting frequencies at which the device under test experiences excursions two times larger

than non-resonant excursions.

8.4.3 THERMAL SHOCK

Non-operating: -40 (+/-5) to +70 (+/-5) degrees Celsius, transition time not to exceed 5 minutes. Duration of exposure to temperature extremes will be 20 minutes**.**

8.5 MTBF and Quality Data

8.5.1 MTBF

The life requirement shall be met the following condition. And the environmental temperature is assumed to be 25 degrees Celsius.Normal operation (at the rated input/output): 150,000h.

9 Regulatory Agency Requirements

The power supply must comply with all regulatory requirements for its intended geographical market as computer server of Information Technology Equipment.

The power supply must meet all regulatory requirements for the intended market at the time of manufacturing. This power supply shall have below certificates for ITE category:

- UL
- C-UL
- TUV
- CCC
- CB
- CISPR Class B (920P-1R Class A)
- FCC Class B (920P-1R Class A)
- CE criteria B for power supply itself
- RoHS (Full ROHS lead free 6/6)
- Efficiency 80plus platinum Single Output
- Immunity to meet ITE machine category on EN61000-4-X

The power supply itself meets class A with 6 dB margin of EMI limits for CE, FCC, CISPR tested with full output resistance loading, and certificated with CE compliance.
The power supply, when installed in the system, shall meet immunity requirements specified in EN55024. Specific tests are to be EN61000-4-2, -3, -4, -5, -6, -8, and -11. The power supply must maintain normal performance within specified limits. Conformance must be designated with the European Union CE Marking. Specific immunity level requirements are left to customer requirements. Criteria A of EMI immunity regulatory.

10 acoustic noise and Fan Speed Control

Acoustic noise limitation: The acoustic noise level of PS stand-alone operation including stand-by operation must be less than 15dBa without fan. The vendors need to provide the test data of acoustic noise without fan for during DVT, PR stages

When AC plug in, Fans will be on and have minimum speed to cooling power supply to keep normal operating temperature. The power supply will have internally controlled PWM fans. The PWM fans will be thermal controlled by microcontroller. Note that speed transition should be non-linear to reduce perceived noise from fan.

Pin 17 implement a function for system control power fan speed into normal or quiet mode go through power PDB same pin to empty pin (was for -5V) output on 24pin or 20pin connector.

5V TTL Low @ pin 17 – Fan operate in quiet mode
5V TTL High or no connection @ pin 17 – Fan operate in normal (default setting)

Fan control speed rule is shown in the attached file below.

PWM Fan Control Design Guideline 0.1.

Fan Speed Control

The power supply will have one internally controlled 28mm or 56mm fan. The fan will be 4 wires PWM Fan controlled by internal temperature and will have a slope of TBD.

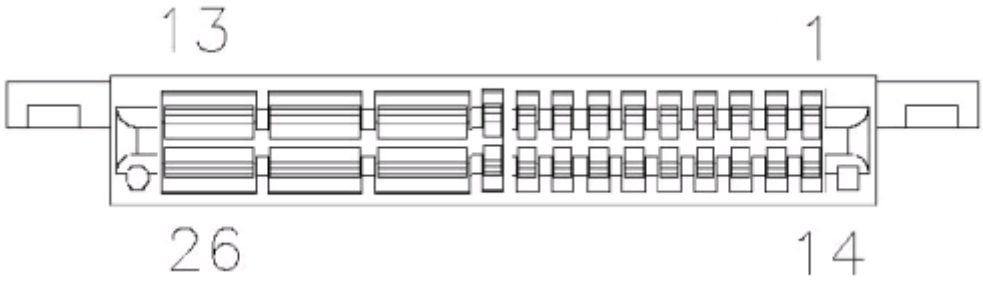
11 Output Connector and Dimension

The power supply will provide a card edge connector compatible with the backplane. See power supply mechanical drawing for dimensions. The power supply connector is a 6 blade (3 pair) and 20 pins (10 pair) edge connection type from Tyco Electronics, Mfr P/N 1489958-1 or FCI P/N 10034908 connector.

Power and Signal Connection

Description	Pin Number	I/O	Active	Pin Length
Ishare	1		Analog	Standard
A1 (address)	2	I/O	High/Low	Standard
A2 (address)	3	I/O	High/Low	Standard
I2C SCL	4	I/O	High/Low	Standard
I2C SDA	5	I/O	High/Low	Standard
PS ON/OFF	6	I	Low	Short (by 1mm)
Spare	7			
DC GOOD	8	O	High	Standard
+12V	9		Power Pin	Standard
+12V	10		Power Pin	Standard
+12V	11		Power Pin	Standard
+12V	12		Power Pin	Standard
+12V	13		Power Pin	Standard
RS GND	14		Analog	Standard
Spare	15			
12V RS GND	16		Analog	Standard
Fan Control	17	I	High	Standard
DC Return	18		Power Pin	Standard
5Vsb CO	19		Power Pin	Standard
5Vsb CO	20		Power Pin	Standard
DC Return	21		Power Pin	Standard
DC Return	22		Power Pin	Standard
DC Return	23		Power Pin	Standard
DC Return	24		Power Pin	Standard
DC Return	25		Power Pin	Standard
DC Return	26		Power Pin	Standard

.**Note:** The signal pins on the power supply connector will be gold plated to 30 microns.



The power dimension is same current PWS-801-1R

PWS8011R.pdf

Barcode:

920P-1R…… P9211CYWWRMSSSS.

12 Assembly Process

Supermicro confirms the assembly process, test process. If they have a problem, Supermicro requests to improve the problem.

13 Safety

13.1 Dielectric Strength Testing (Hi-pot)

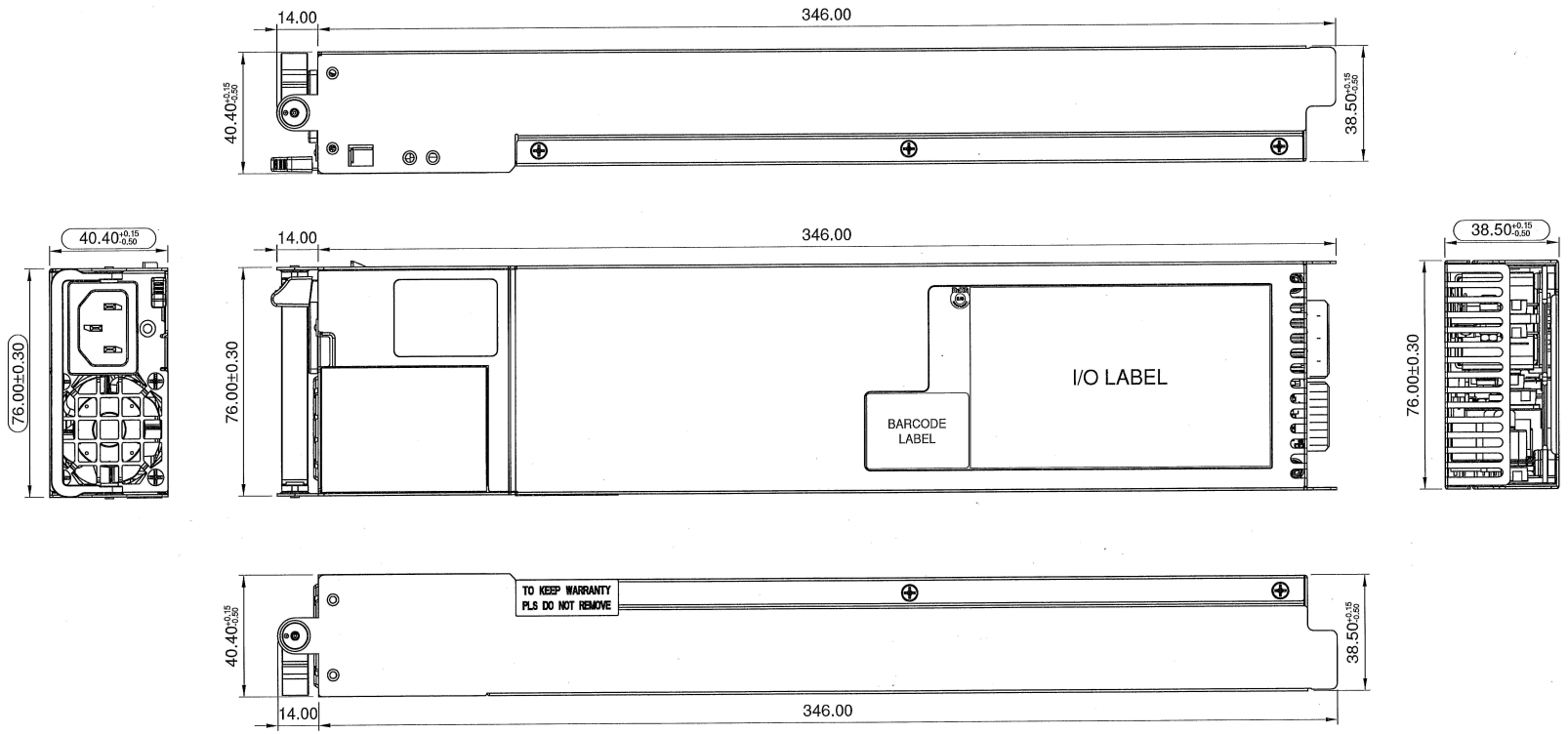
All units must pass a 1500VAC line to ground/chassis hi-pot test. The voltage must be maintained at that level for a minimum of 1 second without failure.

13.2 Ground Continuity Testing

All units must pass a ground continuity test with less 0.1 Ohm from the ground (third wire) input pin to the chassis.

REV.	Description	Modify By	Modify Date	Amendment basis ECR NO.
A0	Release	Kevin	2010.01.25	-
A1	-	-	-	-
A2	-	-	-	-

NOTES:
1. INTERPRET DIMENSIONS PER CNS.
2. DIMENSIONS NOT SHOWN ON DRAWING SHALL REFER TO A GENERAL TOLERANCE.
3. ALL EXPOSED EDGES MUST HANDLING REQUIREMENTS SPECIFIED IN UL 1439.
4. MATERIAL SURFACE AND INTERIOR SURFACE OF HOLES TO BE FREE OF OIL, NICKS, BURRSS AND RESIDUE.
5. ALL COMPONENTS AND THEIR MANUFACTURING PROCESS SHALL BE FULL RoHS.
6. DIMENSIONS WITH SYMBOL " ( ) " ARE CRITICAL, MUST BE INSPECTED EVERY SHIPMENT.



COMPUWARE	COMPUWARE TECHNOLOGY CO., LTD.								
Model: CPR-9211-1M1LF				Drawing No.: CPR-9211-1M1LF(V1.0)					
Title: CPR-9211-1M1LF OUTLINE DRAWING				Part No.: CPR-9211-1M1LF(V1.0)					
CTO	Approved	Reviewed	Drawing	Material	Finish	Unit	Scale	VERSION	
Sevy	Brian	Eric 2010.1.25	Tom 2010.1.25	-	-	mm	1:1.5	N/A	

TOLERANCE	
Length (mm)	
15Down	±0.10
16-50	±0.15
51-100	±0.20
101-300	±0.30
301-600	±0.40
Angle	±1.00°